RELIABILITY OF SOLDER JOINTS: WILL VOID FREE VACUUM SOLDERING HELP?

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Abstract
Rapid incorporation of low cost, small footprint, and high efficiency BTC components with a large thermal plane and leadless terminations presents numerous challenges to the PCB manufacturers. Customers are demanding and many manufacturers are struggling to reduce voiding in the BTC assemblies to levels being asked for. Vacuum soldering has always been one answer for voiding.

Expensive equipment modification was introduced and proposed to reduce voiding. Many papers were published highlighting that, depending on application, voiding levels have little or no detrimental effect on solder joint reliability. Overall industry is struggling to come to consensus on the genuinely tolerable levels of voiding and different mitigation strategies.

This investigation has focused on direct comparison of two different alloys assembled both using conventional reflow process and vacuum soldering. Thermal cycling testing at -40C/+125C with 30 min dwell time was used to evaluate reliability performance of two different sizes of QFN assemblies. Test vehicle chosen for this work had 6 copper layers and includes two different sizes QFN components (MLF100 and MLF52). In all cases the same commercially available solder paste was printed with the same stencil (5 mil). Matching reflow profiles in conventional and vacuum reflow were used. Voiding of all assemblies were assessed. As expected, a drastic reduction in voiding was measured for vacuum soldered assemblies. Very unexpected reliability results were observed, highlighting potentially unintended consequences associated with vacuum soldering and void-free assembly.

Key words: solder joint reliability, vacuum soldering, voiding.

Introduction

Discussions regarding voids in Surface Mount Technology (SMT) assemblies continues at all levels and for different market segments. The amount of voiding can vary within an assembly depending on solder paste formulations, used solder alloys, board design and board and component surface finishes, stencil/apertures design as well as reflow profiles. That is by no means an exhaustive and complete list of factors affecting voiding. Most discussion on voiding concentrates on mechanical and thermomechanical reliability performance of the devices. No agreement exists on the effect of voiding on thermomechanical reliability of solder joint assembly. Effect of voiding on thermal and electrical conductivity of the assembly could be assessed based on calculation, but it is not that straightforward for reliability assessment. Speculation that voiding affecting solder joint cross-sectional area could result in reduced solder joint reliability, fear that voids increase internal stress and acts as a crack propagation path. At the same time there are claims that voids could act as crack termination spots and stress relievers. Also, there are some claims that voiding could result in more flexible solder joints with higher stand-off which results in more reliable solder joints. Numerous papers have been published highlighting positive and negative effects of voiding.

Industry agreed on classifying and identifying voids into six major types [**1-3**]. In this study the focus is on the processing macro voids. Those voids are not board design or surface finish related and could be easily observed during ordinary X-Ray inspection. It needs to be pointed out that other types of voids could have significant impact on the system reliability. These will not be addressed in this study as they are not considered to be present in this experiment.

There are multiple standards IPC-A-610G, J-STD-001G and IEC 61191-2 **[4-6]** describing the upper limits of voiding for various components. Typical, well controlled manufacturing process, with commercially available solder pastes and reliable surface finishes, produce assemblies with voiding levels within specified limits. Overall, there is no consensus on allowed voiding levels for typical SMT, only for high thermal application when size and location of the void could affect functionality.

With increasing reliability performance requirements and power management, more attention is focused on void effect on thermal and electrical performance of Bottom Termination Components (BTC) like QFNs. The market demand is for void reduction under thermal pads of QFN components at all cost. Unlike QFPs where there are leads and BGAs where there are bumps, BTCs provides very limited, low standoff height. The pad in the center of the BTC primary function is to insure heat dissipation. It was reported **[7]** that low voiding is important for decreasing the current path of the circuit to maximize high

speed and RF performances. Since there is such a large surface area and no fixed standoff to allow the volatiles to escape, these gasses may become entrapped and cause excessive void formation. Device design and size are limiting the ability to affect voiding from stencil aperture design. But reflow atmosphere (introduction of vacuum reflow) could influence voiding of the devices. Customers demand on void reduction across all assembly and device types pushes for new low voiding solder paste chemistry development, introducing preforms for problem components, implementing new approaches and methods of assembly. In recent years more and more reflow equipment manufacturers are introducing vacuum capability to address customer requirements.

Experimental Procedure

As a part of a larger project, reliability of BTC solder joints built using different alloys were evaluated. **Figure 1** shows the board designed for thermomechanical reliability of BTC and BGA devices. Test vehicles were designed to have integral copper 'loading' representative of production PCBs and component types. Copper OSP was used as a surface finish. Thickness of the PCB was 1.6mm (+/-10% tolerance). Board was designed to have 6 layers, 4 inner layers to be copper with square pattern or cross hatch to give approximately 60% copper/40% space (to approximate functional ground planes). 1 Oz copper was used in the inner layers.

Effect of voiding level on BTC assembly reliability was assessed. Conventional reflow and vacuum reflow in a batch vacuum oven were used. The soak reflow profile increased temperature at a rate of 1°C/s until up to reaching 170°C before slowing to a rate of 0.5°C/s up to 200°C allowing more time for flux to activate and reduce the volume of volatiles. The test vehicle was subjected to 65 seconds above liquidus (TAL) with peak temperature on the test vehicle reaching 250°C. Air reflow atmosphere in conventional reflow was used. Profiles in vacuum and conventional reflow were matched. **Figure 2** shows overlap of both profiles. For vacuum soldering, vacuum was introduced as soon as the solder got molten, and the vacuum level was 30mBar for 30 seconds.

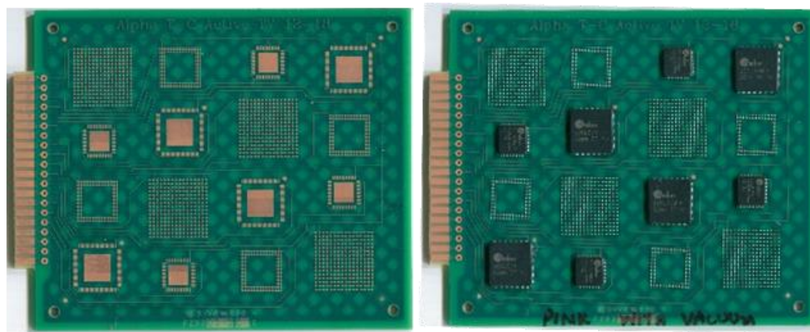


Figure 1. Image of the PCB test vehicle (TV) and some of the components used in this experiment

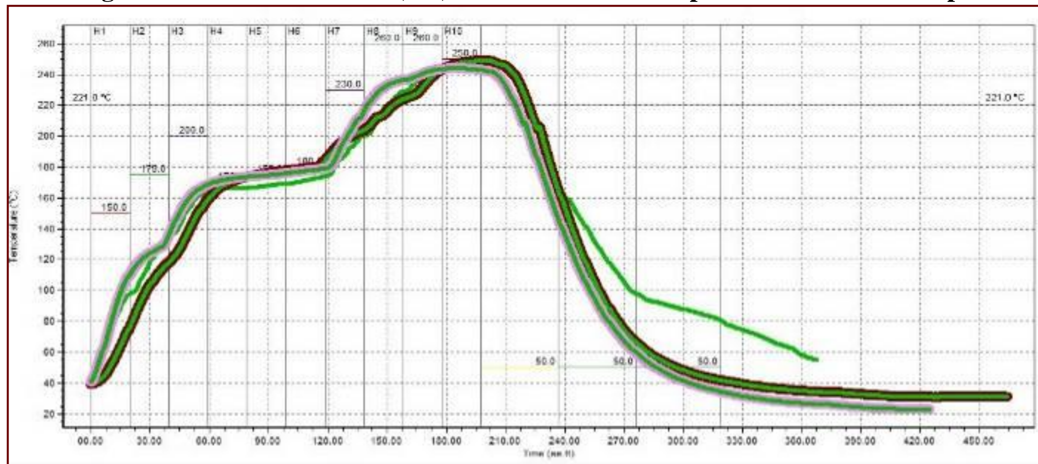


Figure 2. Reflow profiles using in this study. DARK GREEN-vacuum and GREEN- conventional reflow.

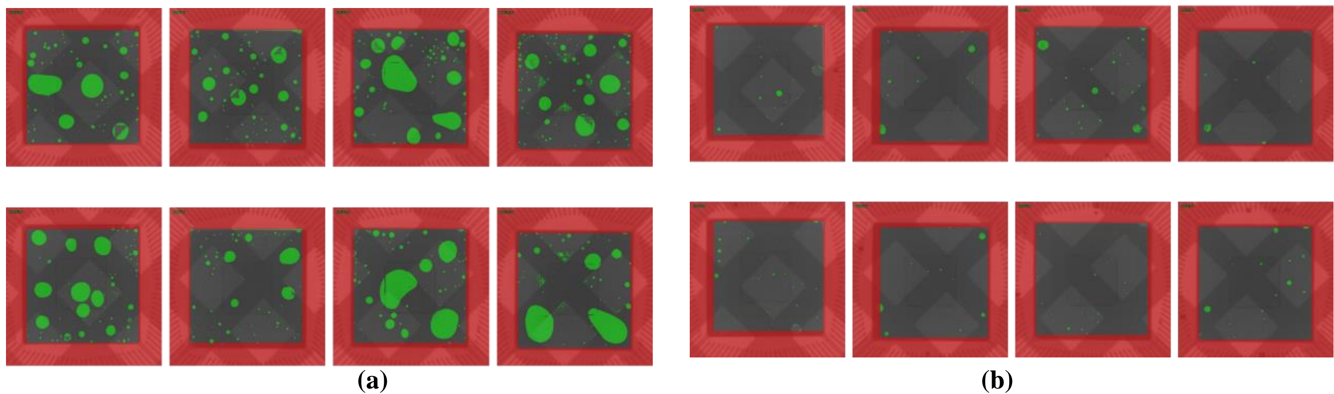
X-Ray analysis was performed on all assemblies to assess voiding prior to thermocycling. Boards were subjected to thermocycling at -40°C to +125°C with 30 min dwell time. Slow transition rate and temperature dwell were chosen to be 30minutes, which offers the toughest challenge i.e., allows longer time for plastic deformation to occur in the solder joint. Resistance values of the I/O connections of the assemblies were monitored. Increase in resistance was indicative of solder joints

failure/cracking. All assemblies were tested for up to 3000 cycles. Increase in resistance by 20% in five consecutive measurements was considered to be a failure. Data was tabulated and analyzed.

Microstructural evaluation of the solder joints was performed before and after thermocycling. IMC layers at both (component/solder and solder/board) interfaces were measured. X-Ray void analysis of the solder joints before and after thermocycling showed very little to no variation.

Results and Discussion

X-Ray images shown in **Figure 3** clearly demonstrate difference in void level for assemblies built using conventional reflow profile and vacuum soldering. No variation in solder paste chemistry or aperture designs were used, just the difference in atmospheric pressure while solder was molten (air vs. vacuum). As expected, assemblies built in conventional reflow showed (**Figure 4**) that the larger component (MLF-100) has higher voiding compared to the smaller component (MLF52). As to be expected, in all cases assemblies built with SAC+SbBiNi produced slightly higher voiding compare to SAC305. Overall voiding was in 10-25% range/ In the case of vacuum soldering, much lower voiding levels were achieved for all assemblies: 0.5-2%. Another similar trend was also observed: smaller component, less voiding.



(a) (b)

Figure 3. X-Ray images of the MLF100 assemblies build using (a) conventional reflow process and (b) vacuum reflow process

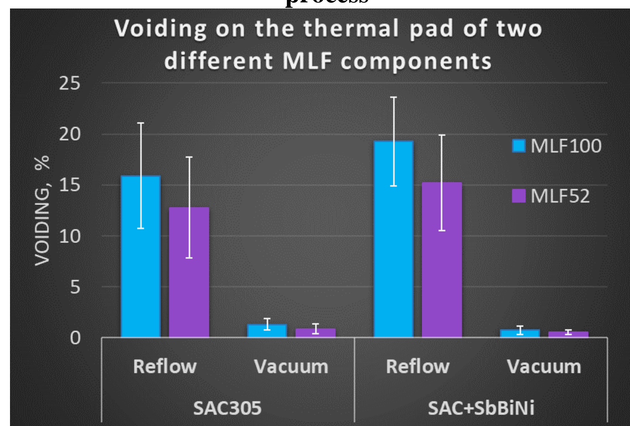


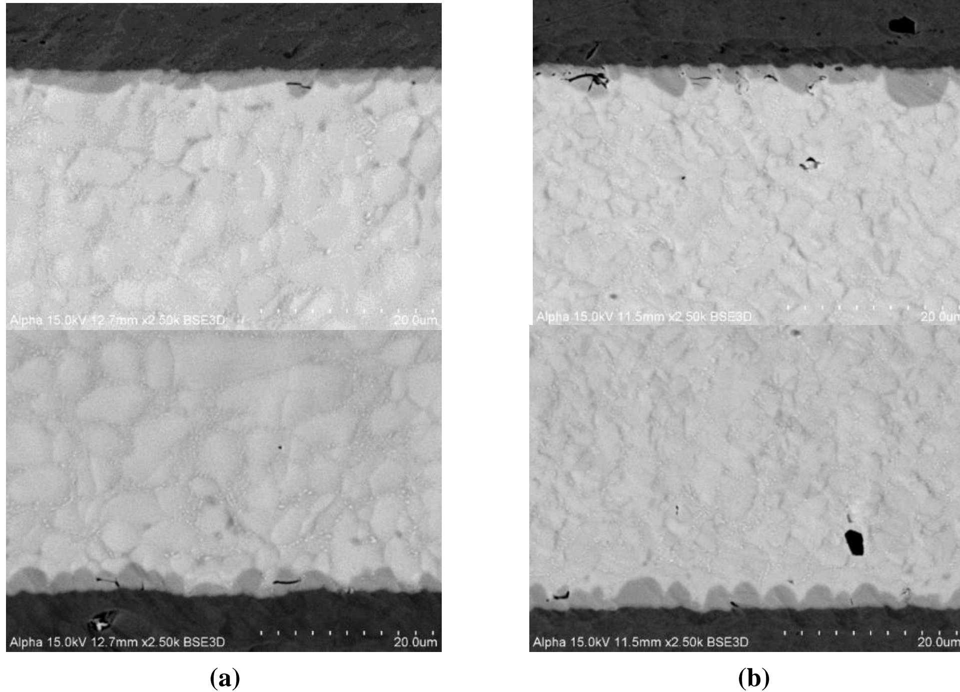
Figure 4. Void Analysis of the assemblies

Microstructural and interfacial evaluation of assemblies built in conventional reflow and in vacuum was performed. In both cases for SAC305 and SAC+SbBiNi (**Figure 5** and **6**) there were very little or no differences in microstructure or IMC layer at ether interfaces. Note, solder paste chemistry, board and stencil design, temperature profile during reflow were identical, just pressure was different during TAL. Microstructural evaluation of assemblies before and after thermocycling was performed. **Figure 7** shows comparative SEM images of the cross section SAC305 and SAC+SbBiNi as assembled component's thermal pad and after 3000 cycles exposure. Some grain growth was observed, bulk intermetallic and precipitates growth was observed especially in SAC+SbBiNi. As expected, the reflow method did not affect initial microstructure or rate of precipitate or grain growth because of thermocycling.

A big difference was observed in IMC layer between SAC305 material and SAC+SbBiNi **Figure 8** shows that there might be not a big difference in total thickness of Sn/Cu IMC at the interface for both alloys, but the type of IMC layer and morphology is slightly different. Total thickness and individually Cu_6Sn_5 and Cu_3Sn were measured. Thickness of IMC layers are shown in **Figure 9.** As reflowed, there were not a lot of difference between SAC305 material and SAC+SbBiNi Sn and between

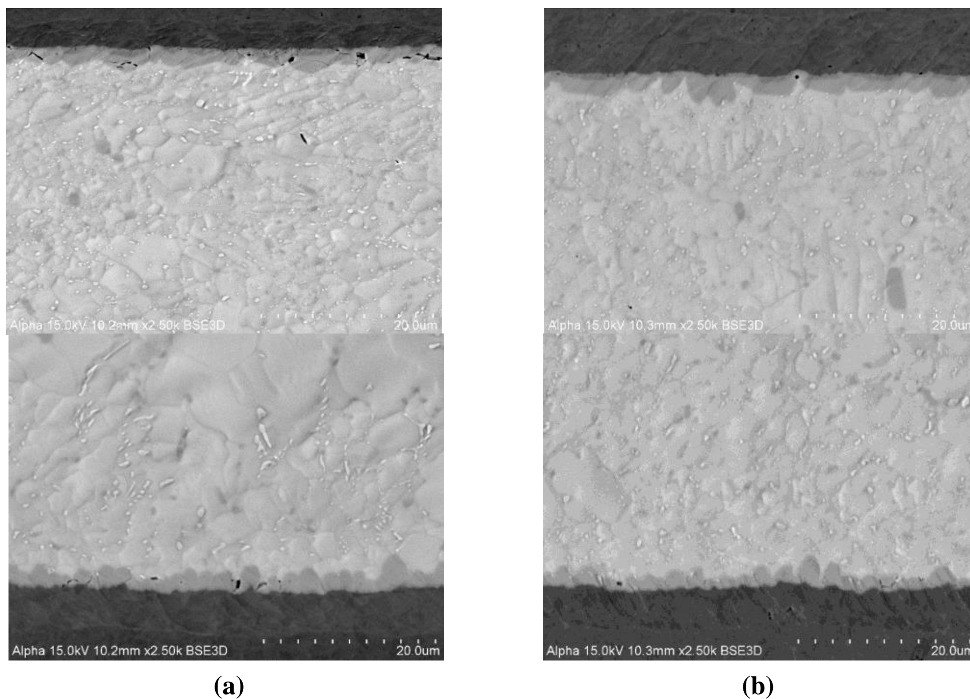
assemblies reflowed in air and vacuum. Also, both alloys are high silver alloys and were expected to have very similar thickness of IMC because reflow profiles were the same. As material was aged (exposure to higher temperature during thermocycling) the thickness and morphology of the IMC was measured. Alloying additions to SAC+SbBiNi alloy change the kinetics of IMC growth, effectively making the IMC layer slightly thinner and having smaller grains while SAC305 showed thicker, larger grains.

Results of the thermocycling is shown in **Figure 10**. As mentioned earlier, resistance increase by 20 % in five consecutive measurements for specific component was considered as a failure. Results are shown in stacked dots, those failure did not happen at exactly the same time, it is a data compression artefact of the graphical method. Original expectation was to have better performance of the assemblies with no voiding, but it shows that voiding was beneficial especially in SAC305 alloy



(a) **(b)**

Figure 5. SEM images of the cross sectioned SAC305 assemblies (a) conventional reflow and (b) vacuum soldered



(a) **(b)**

Figure 6. SEM images of the cross sectioned SAC+SbBiNi assemblies (a) conventional reflow and (b) vacuum soldered

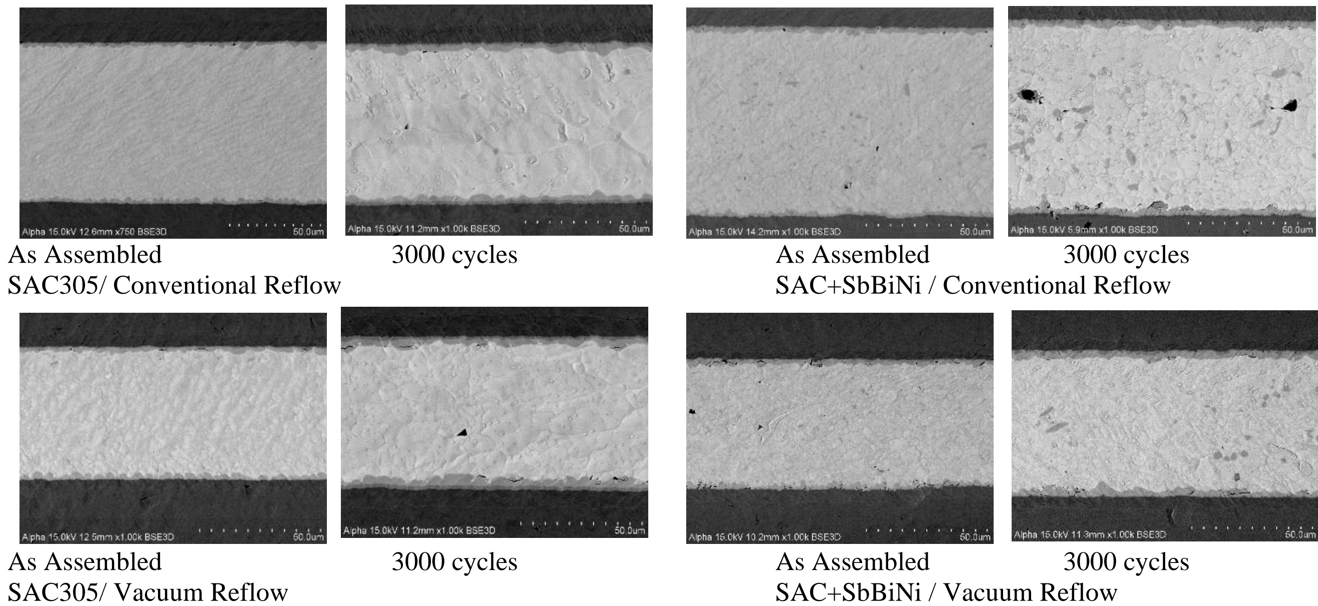
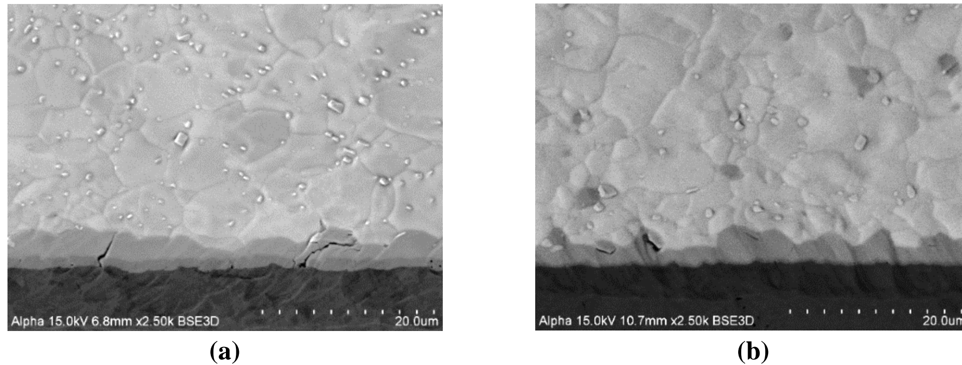


Figure 7. SEM images of the cross sectioned thermal pad on MLF100 component before and after thermocycling.



(a) **(b)**

Figure 8. SEM images of the cross sectioned thermally cycled assemblies (a) SAC305 and (b) SAC+SbBiNi

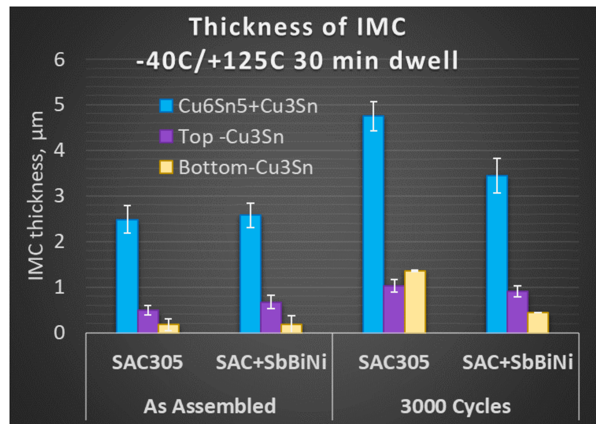


Figure 9. Measured IMC layer thickness on various assemblies before and after thermo cycling.

Further analysis of assemblies was undertaken to establish the root cause of the faster degradation of the assemblies with no voids. Cross sectioning of the BTC components was done and bondline thickness was measured (**Figure 11**). Not surprising, components with voids had thicker bondline. The same paste amount was printed and reflowed, but voids occupy some of the finished reflowed volume, resulting in increased bondline. Typically, it was measured 15 to 20 microns difference in bondline between assemblies build in conventional reflow vs. vacuum reflow.

In some of the previous studies, it was observed that depending on the alloy (**Figure 12**), development of cracks and delamination will increase as number of cycles increases at different rates, but the rate of failure irrespective of the alloy was dependent on the bondline thickness. **Figure 13** shows the increase in thermal conductivity of the assembly as a function of number of cycles. For the same alloy degradation would be slower for thicker bondline compared to the thin one.

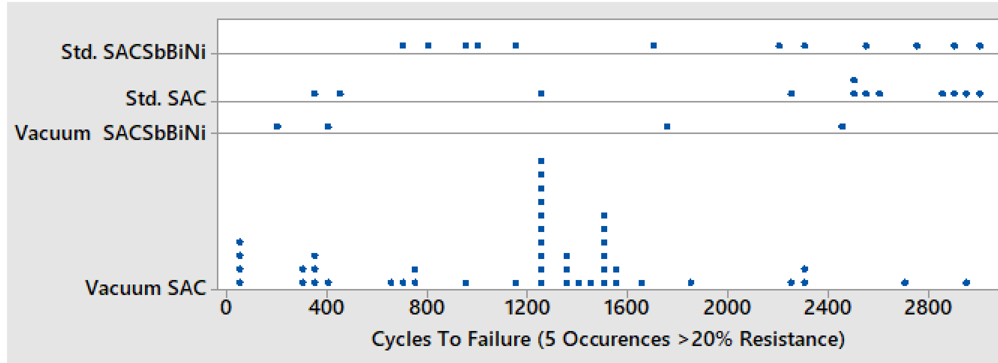


Figure 10. Thermocycling Data.

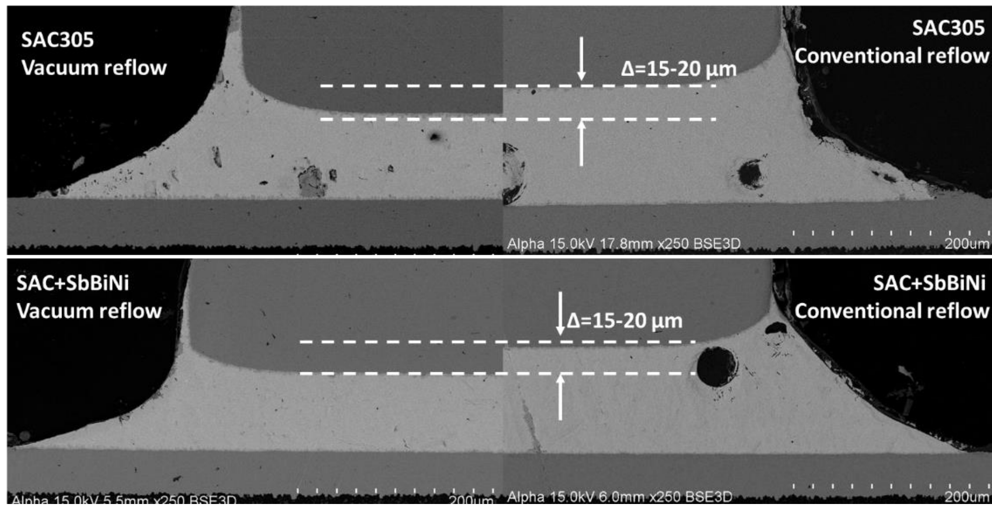


Figure 11. SEM images of the cross sectioned leads on MLF100 components assembles using conventional reflow and vacuum reflow process.

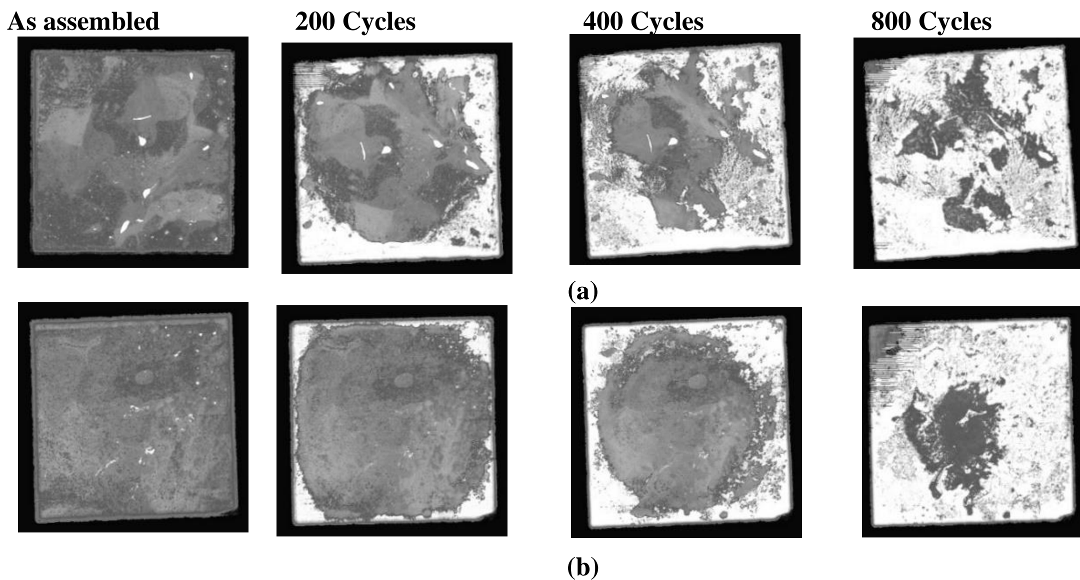


Figure 12. CSAM images of the die attached components assembled using (a) Sn3.5Ag and (b) SAC+SbBiNi alloys during thermocycling.

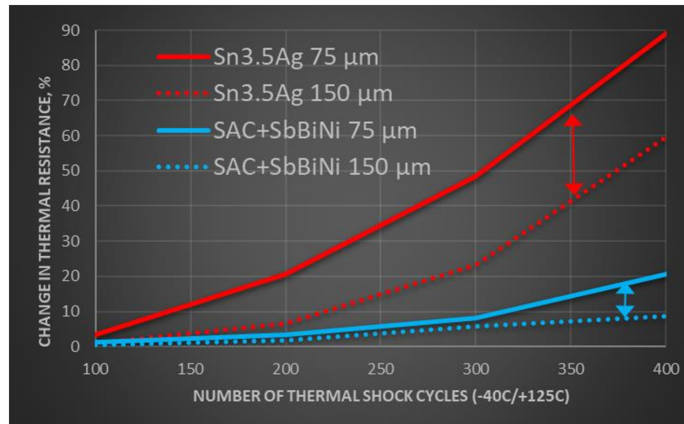
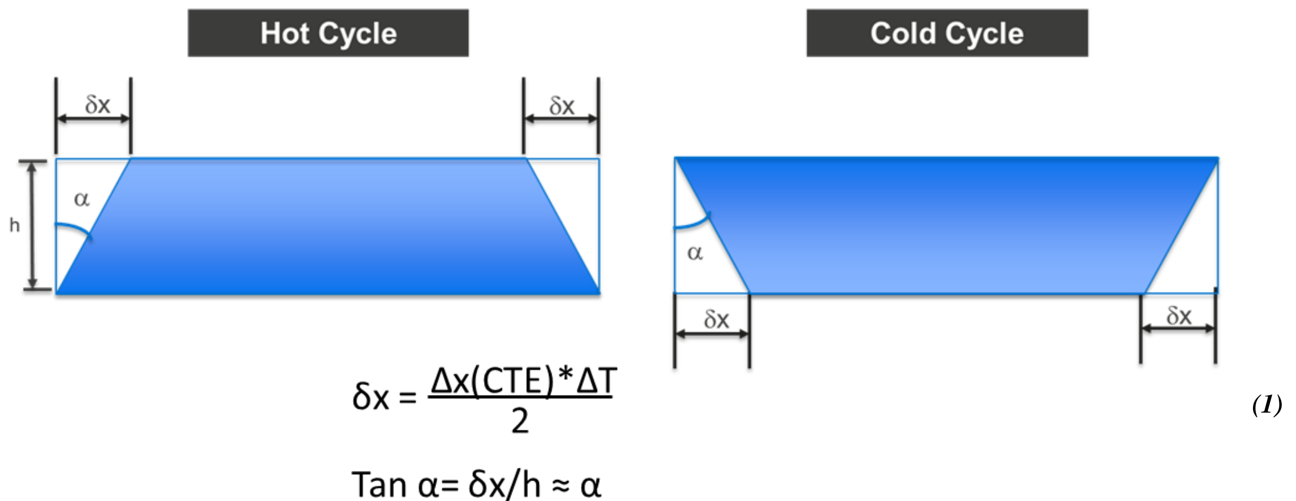


Figure 13. Change in thermal conductivity of the assemblies as a function of number of thermal shock cycles.

Those earlier observations resulted in development of a simple mathematical model for displacement at test temperatures (-40°C and +125°C) for various thickness of the assemblies (**Figure 13**) with identified component size and CTE for board and substrates. If one assumes that board CTE is about 14-17ppm/^{o} C and ceramic components CTE is anywhere between 3 to 8 ppm/^{o} C (depending on the design), during cold cycles (-40°C) and hot cycle (+125°C), contraction or expansion of the board and component would be different (***equation 1***). The amount of displacement (***δ x***) will be dependent on difference in CTE (Δx(CTE)) and the height/bondline (***h***) or distance between component and a board.



$$\delta x = \frac{\Delta x(CTE) * \Delta T}{2} \qquad (1)$$

$$\tan \alpha = \delta x / h \approx \alpha$$

Figure 13. Schematics of Shear Strain calculation as a function of temperature and CTE mismatch.

The calculation of the displacement in x direction and at the diagonal for MLF100 component (12x12mm body size) with assumed CTE of the board to be 17ppm/^{o} C and component CTE to be 3ppm/^{o} C are shown in **Table 1**. Measured bondline difference of 20 microns would result in almost 30% change in overall displacement resulting on higher stress. Increased stress level due to larger displacement and higher shear strain, could contribute to faster degradation of the assembly with a thinner bondline.

Table 1. Calculated Shear Strain for MLF100 component

Height (h) in mm	Shear Strain at temperature (C)			
	in x direction		in diagonal direction	
	-40 °C	125 °C	-40 °C	125 °C
0.07	-0.078	0.120	-0.110	0.170
0.06	-0.091	0.140	-0.129	0.198
0.05	-0.109	0.168	-0.154	0.238

Summary and Conclusions

This experimental work was designed to hopefully confirm that the absence of voids both under the central termination and signal (I/O) positions of QFN type devices was beneficial to the assembly's thermomechanical performance. However, it generated what at first looked like anomalous data contradicting this. Further investigation of the assembly however showed an unintended consequence of void reduction and that was a reduction in device buoyancy leading to a reduced 'bond line' layer of solder.

From both previous experimentation and anecdotal data from real assemblies tested in production it is known that a 20µm change in the standoff height of a QFN can have a significant effect on the thermomechanical performance of the device. This is shown in the calculation by an increase in displacement (x/y) (shear strain) as the stand-off decreases (z).

What appears to be illustrated is that the more creep fatigue resistant SAC+SbBiNi alloy is more capable of tolerating this reduction in bond layer thickness which is commensurate with data from other experimentation on die attachment.

This leaves the possible conclusion that voids on central terminations of this specific type of device may be more beneficial than first thought simply due to a buoyancy effect driving a greater device standoff.

The work presented in this study, demonstrates the advantage of using vacuum reflow in creating almost void-free Bottom Termination Components (BTC) assembly, however, challenges the theory that all levels of voiding are bad. Results presented herein suggest that some level of voiding can be beneficial in enhancing thermal mechanical performance of a resulting assembly. The presence of minor levels of voiding provides higher standoff height appears to attenuate the shear strain generated in the I/O connections of the device from the CTE mismatch of the PCB and component. This is evidenced by the lower rate of failure on the bottom terminated components used for this study when higher levels of voiding were observed during the air reflow process. Additionally, there was no significant difference in thermal conductivity observed between the higher and lower voiding level packages. Further studies would be required to determine at which point voiding might become detrimental, but evidence suggests near zero voiding may not be the most practical solution.

Acknowledgement

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