The Total Environmental Solution for Any-layer HDI Production

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Abstract

Copper Via-Fill application in acid copper plating of PWB grows significantly due to the booming of smartphone and tablet PC application in which the PC board demand of HDI complexity increases. The "any-layer" design is widely adopted in layer count reduction whereas the circuit density is increased due to more freedom in designing the circuitry. This kind of build-up process required 100% blind micro-via fill up in every single layer and stack up for interconnect. The challenge of this design is the zero tolerance of dimple as well as minimal copper build up for ultra fine-line circuit formation. The latest development of via-fill has set the new standard of zero dimples with copper build up less than 10 um. No copper reduction is required, even for the ultra-fine line etching process in which the circuitry goes down from 20/20 µm L/S to 15/15µm L/S. Another challenge of the process is prolonged plating cycle time. This paper will illustrate an advanced super-filling technology which was developed in the combination with green PTH alternative; conductive polymer direct metallization. The direct via-filling on conductive polymer becomes possible which could minimize the use of copper as well as shorten the total process cycle time by more than 50%. The extraordinary coverage of conductive polymer over glass and resin surpass the traditional electroless copper performance; thus enhance the current flow for via-filling. The mechanism of the specialized additive system over the conductive polymer was investigated. Today's equipment for copper via-fill in PWB industry is dominated by either vertical or horizontal conveyorized system. The hydrodynamic impact to super via-fill performance will also be discussed.

Introduction

When the smart phone was first introduced to the market in 1990s by IBM [1], the phone call in combination with the functionality of personal computing turn to a new era of mobile communication. IBM had developed new fabrication methods including build up technology, laser processing, copper via plating and fine-line patterning, etc. for the board manufacturing. Since then, the smart phone OEMs recognized, apart from functionality, the next critical components of device are the weight and size. There are more innovations every year in PWB for higher I/O but smaller size. High density interconnect (HDI) is a necessary part of such device and the density of semiconductor was gradually increased every year that also drive the miniaturization of PWBs. Traditional HDI structures feature micro-via in build up layers and the micro-via in adjacent build up layers are staggered [2]. There is a constant struggle to increase features while decreasing the size of area array packages. The result is increasing interconnect density and decreasing micro-via size. Although this has created some challenges for fabricators, coreless structures can form staggered as well as “stacked” micro-vias which enables designers to connect two points of different layers with shortest conductive path to reduce electric signal losses and number of layer counts. The "any-layer" in via-hole design (or called ELIC/ALIVH) is widely adopted in most of the large PWB suppliers in smart phone application that give the highest value and margin of PWBs [3]. Since any-layer is a kind of build-up process which required 100% blind micro-via fill-up in every single layer, the consumption of both additive and

copper is very high. In addition, the circuit density for cell phone boards from 50/50 µm L/S has come down to 35/35 µm. This trend challenges the fabricator in plating distribution in semi-additive process or etching uniformity in normal subtractive process. The PWB companies were now expected to break-through the density of 15/15 µm in line/space and this challenge the manufacturability of most fabricators in controlling the tolerance and quality assurance even further.

Via fill Process Design Approach

Electrolytic copper plating has been used extensively in different level of electronic packaging industry from semiconductor to board level. The design of the via-fill product should ideally maximize the via-fill efficiency by reducing both dimples and copper over plating at the surface for fine-line capability. One way to achieve this is to fill up the blind via's rapidly without overburden of copper on surface. That is the key objective of the latest development. Reducing the absolute copper thickness and variation in thickness will improve etching uniformity, which is critical for fine-line patterning. In addition, today's equipment for electroplating in PWB industry mainly horizontal and vertical conveyorized typed. Both of them are in favour with inert anode application.

The current development of copper via-fill solution considers a complete system approach (chemistry and equipment design) for the efficient plating of blind micro-vias with minimal equipment setup and highest productivity under a very short plating cycle. Figure 1 shows the comparison between traditional via-fill process with the proposed innovative process design.

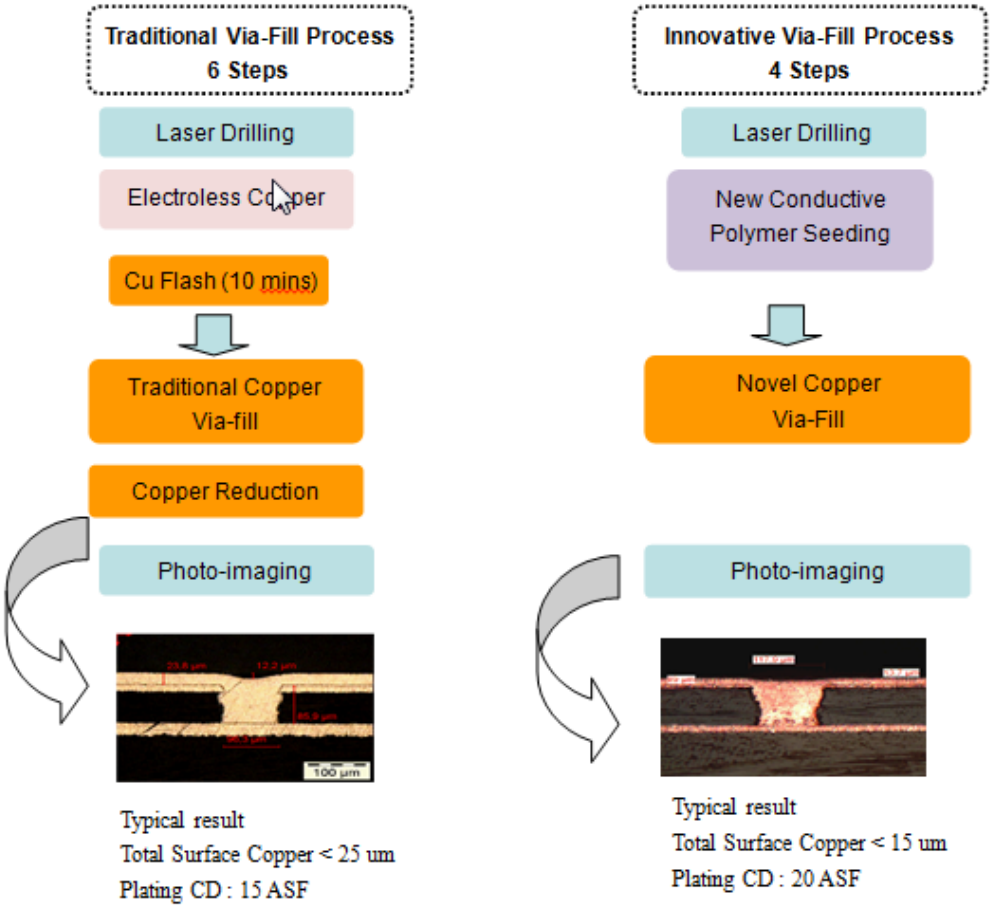

Figure .1 Process Flow comparison of traditional and innovative copper via fill process

The innovative via-fill process has only four steps with elimination of the two time consuming process, copper flash and copper reduction. The filling speed has been improved. This enables 50% of total cycle time reduction. The usage of copper will be reduced by 40%.

Mechanism of the novel copper via fill

Conventional copper plating additives used for micro-via filling typically contain at least two or three components, such as suppressor, accelerator and leveler. These additives create a synergy to perform via filling by bottom up deposition of copper in the micro-via, follow by surface leveling to make it flat or minimal dimple or bump. Unfortunately, copper is also deposited simultaneously on the board surface during plating. This process is shown in Figure 2. In this method, controlling the additives ratio within a very tight window is the key to acceptable via fill performance.

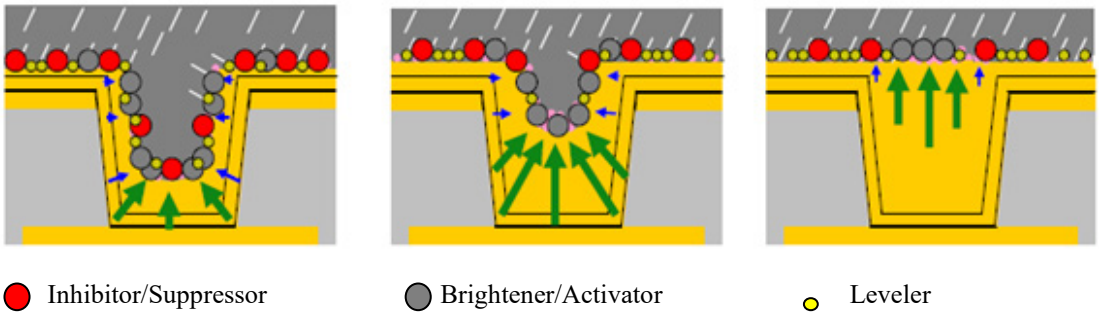

Figure 2. Via fill mechanism

On the other hand, the new proposed solution with conductive polymer layer as a seed layer overcomes some of these challenges and provides an effective and green solution. Conductive Polymer System provides an excellent seeding of copper that give a continuous current flow for via-filling to eliminate void.

The plating chemistry for the new process contains both inorganic and organic components. The organic component, which forms a conductive polymer layer on the surface of the via is the key advantage of this process. The organic component of the plating chemistry selectively coats the dielectrics only without etch back removal of activated copper. This is shown in Figure 3.

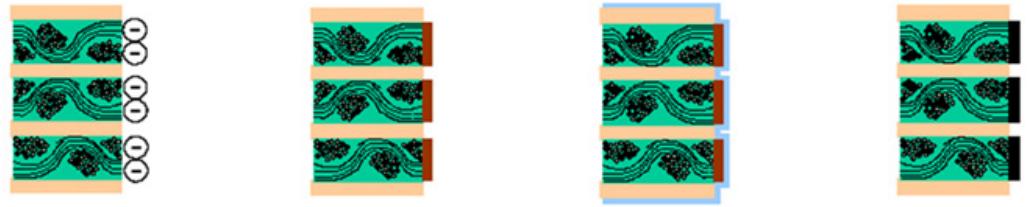

Figure 3. Selective conductive polymer coating

In the conventional two-step process, a copper seed layer is needed to adsorb the accelerator to the plating surface. The main benefit of the one step system is that no seed layer is needed. The principle of plating on conductive polymer is that with a high copper and a low acid concentration the initial copper plating starts relative easy. When a copper layer is formed the adsorption/desorption of the

inhibitor/accelerator system can take place, while it has no significant effect on the conductive polymer.

The factors that influence good via fill for the one step process are, the ratio of the organic additive, hydrodynamics, current profile and insoluble anodes (produces break down products that are also active). These factors are explored in the experimental work, which is described below.

Experimental

Electrochemistry – determine the ratio of organic additive

Selecting inhibitors and accelerators for this development was done in two steps. In the first step an electrochemical approach from the literature was chosen [4]. In this approach the interaction between an inhibitor and accelerator (adsorption/desorption) at the cathode was investigated. In the literature study $Hg/HgSO_4$ was used as reference electrode (in our case Ag/AgCl as inner electrode and sulphuric acid as outer solution) and Pt was used as the working electrode and as counter electrode. The first step involved pre-plating to simulate the plating on copper. The plating conditions for the pre-plating were 20 mA and 100 rpm for 20 sec. However, the primary experiment was done at 10 mA and 1500 rpm for 1000 sec.

The electrochemical study was done by running three different trials. The conditions for each trial are shown in table 1.

Table 1. Electrochemical study conditions

Trial number	Experimental condition
1b	After 250 sec. an Inhibitor and after 500 sec. an Accelerator
2b	After 250 sec. a mixture of Inhibitor and Accelerator was added.
3b	After 250 sec. an Accelerator and after 500 sec. an Inhibitor.

The virgin make up solution (hereafter called VMS) contained 60 g/L Cu, 80 g/L sulfuric acid and 60 mg/L chloride. From each active component 100 mg/L were added. The sequence of addition of each component during the measurement time is described below:

- In the first 250 sec only the VMS solution is measured.
- At 250 sec. the first addition took place.
- In the case a second addition is necessary, the addition followed at 500 sec.

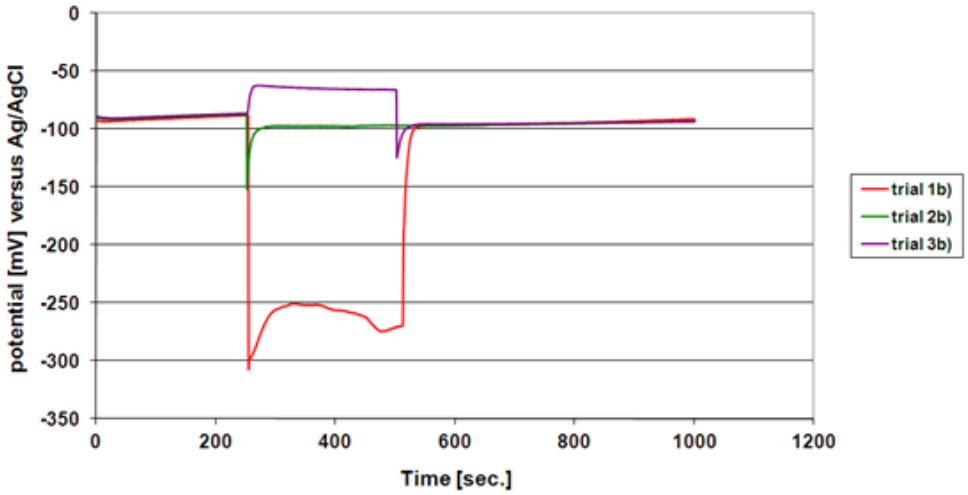

Figure 4. Chronopotentiometry at -10 mA

Figure 4 shows typical results from this trial. As described in in the literature [4] this inhibitor is a type I suppressor. This means accelerator beats inhibitor. Based on the classification of suppressors, a mixture of different types of suppressors was chosen to develop a filling electrolyte.

In the second electrochemical test the adsorption behaviour of the complete electrolyte is determined. For this set of experiments four different currents were chosen according to the plating window. These currents are -1, -10, -20 and -30 mA. At each current setting, the voltage is monitored at 240 sec. The rotating speed for this trial was set at 1500 rpm. Hereby also a pre copper plating was done similar to the first step (-20 mA for 60 sec. at 2500 rpm). An example of the potentials for the VMS solution and the developmental product (CVF-2) is shown in Figure 5.

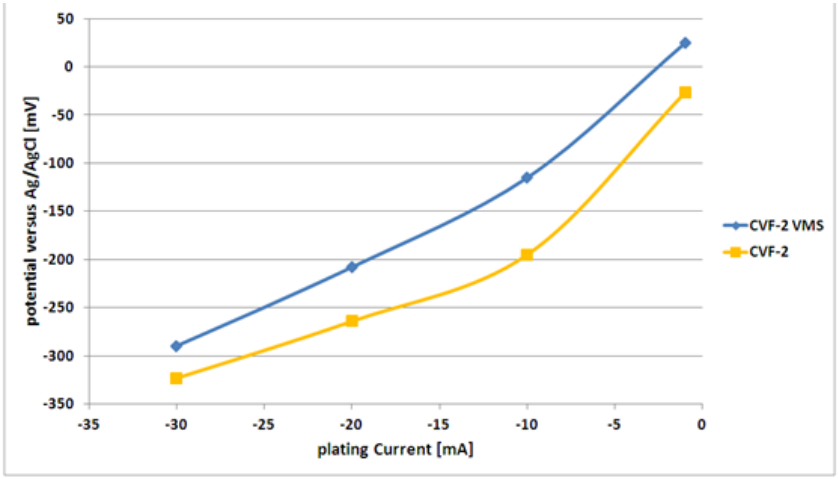

Figure 5. Chronopotentiometry at different Currents

Following these measurement the VMS solution and development solution were examined for potential difference. Through this difference you can see the dependence of the interaction of the complete additive set at the cathode surface in dependence of the current. This means the bigger the potential

difference the higher the interaction of the additive system to the cathode surface. This result is shown in Figure 6.

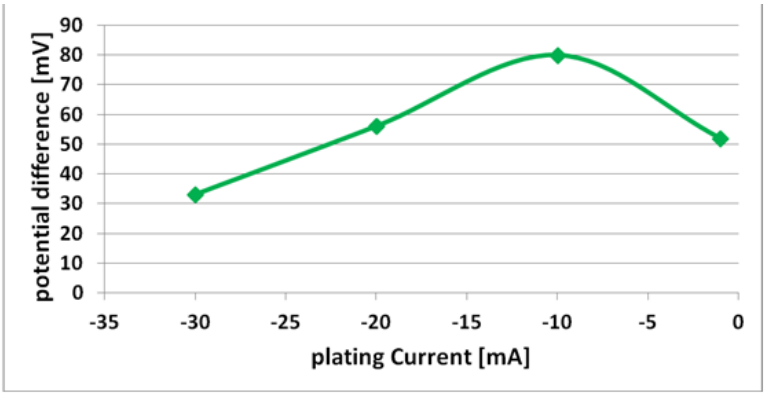

Figure 6. Potential difference between VMS and development solution

We can see from Figure 6 that the additive set had the biggest influence on plating between -10 mA to -20mA. This means the best current density range for plating with the development solution is in the range of 1 to 2 ASD.

In the following different inhibitor/accelerator systems were tested. Figure 7 shows the potential difference for different inhibitors.

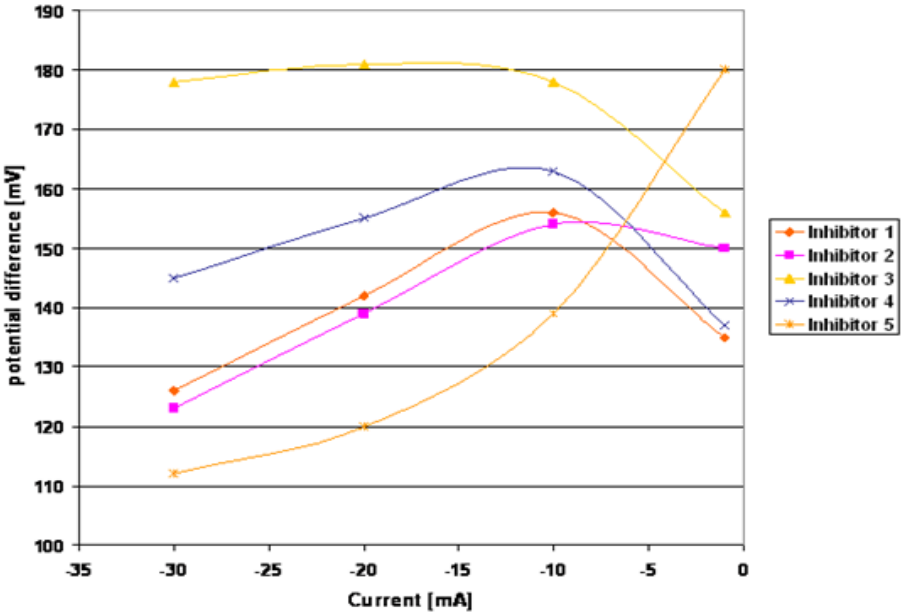

Figure 7. Potential difference for different inhibitor systems to VMS solution

The inhibitor systems 1, 2 and 4 have a similar curve as the development solution (Figure 6). Inhibitor 3 shows conformal filling in the working window of 1 to 2 ASD. This is in good agreement with similar potential difference of around 180 mV from -10 to -30 mA. Inhibitor 5 gives as well filling but the plating time is lower and the overburden is higher.

Process development-VCP Equipment

The electroplating tools are critical part of the via fill process. There are two types of tools used in the industry: vertical (hoist type) or conveyorized plater. The conveyorized platers are generally equipped with high flow sparger or impingement system to increase the solution exchange. The board moving direction is set to be perpendicular to the flow direction. Those systems are particularly suitable for high aspect ratio through hole or deep micro-via as compare to the traditional hoist type tank design. The new via fill chemistry has been tested under different types of VCP configuration.

The test board used in this experiment is shown in Figure 8. It is a 4 layer daisy chain design with 100 and 125 µm via and 250, 300 and 350 µm through hole. Core was 500 µm (20mil) 1/1 with 1080PP with 65% RC. Final HDI layer dielectric thickness was approximately 60 µm. There was no control on direct laser drill as the intention was to check the coating performance if micro-via quality was poor. Example of poor quality is overhang and large glass fiber protrusion.

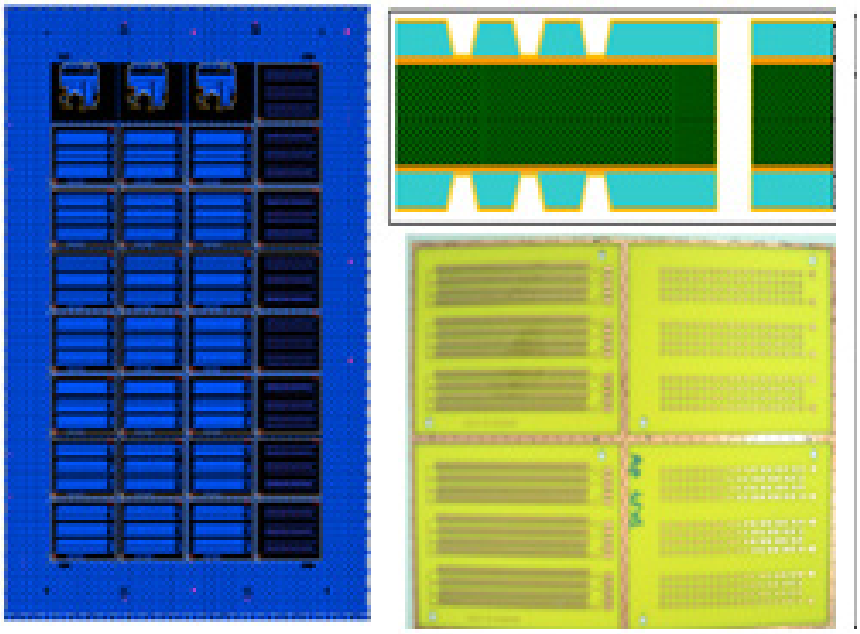

Figure 8. Test board

Plating tool configuration A - Low Flow System

The plating tool configuration which is shown in Figure 9 is designated as “A” type design. It is immersion type, where the boards are moving between two sparger systems on both side. The air agitation is optional; however, the flow rate of the solution could be adjusted from low to high, depending on the preference of the hydrodynamic flow required for the additive. In this set up the additive control becomes the predominate factor for via-filling, rather than solution flooding.

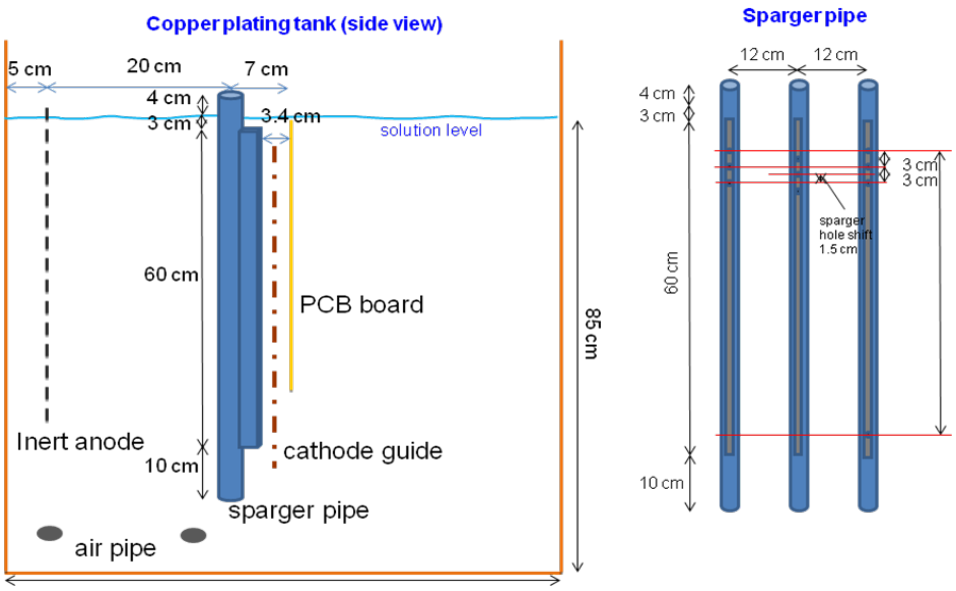

Figure 9. Immersion type plating tool configuration

Plating tool configuration B -High Flow System

"B" Type design is a strong flooding design where the solution level is maintain under a high flow pressure. Figure 10 shows this set up. It helps the solution exchange within the micro via by forced flooding. Via-fill mechanism is dominated by hydrodynamic flow.

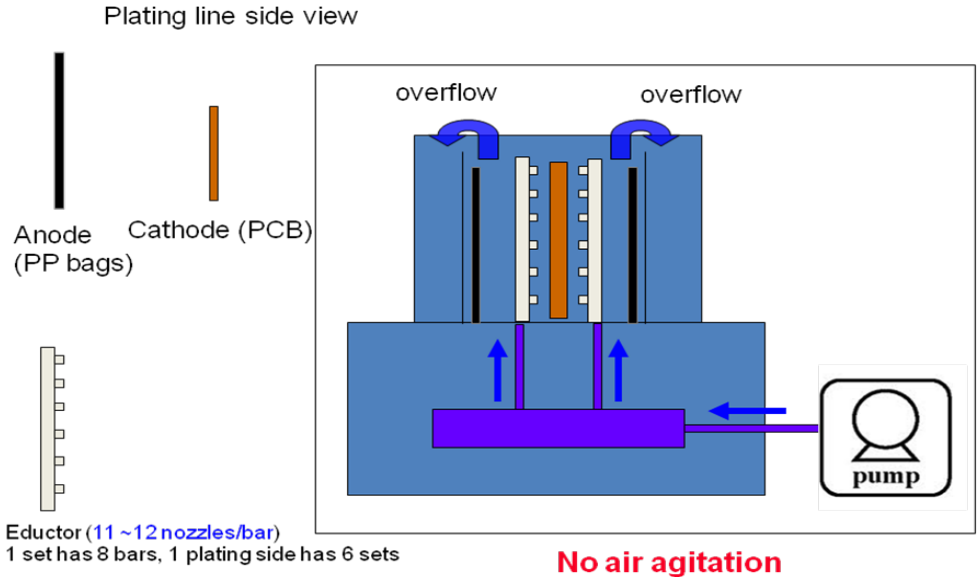

Figure 10. High flow tool system

Hydrodynamic effect

For different aspect ratios Semitool did a theoretical calculation of the solution exchange in the blind micro-via. In the figure 11 the outcome is shown. This theoretical calculation showed as higher the aspect ratio in a blind micro-via is as higher is the diffusion controlled area. Looking at the adsorption and desorption to the cathode surface. There is a much faster exchange of adsorbed additives at the surface in the area with high electrolyte velocity (mass transport driven). In the area of diffusion

control the diffusion speed of each additive is the driving force for the concentration of the additives at the cathode surface.

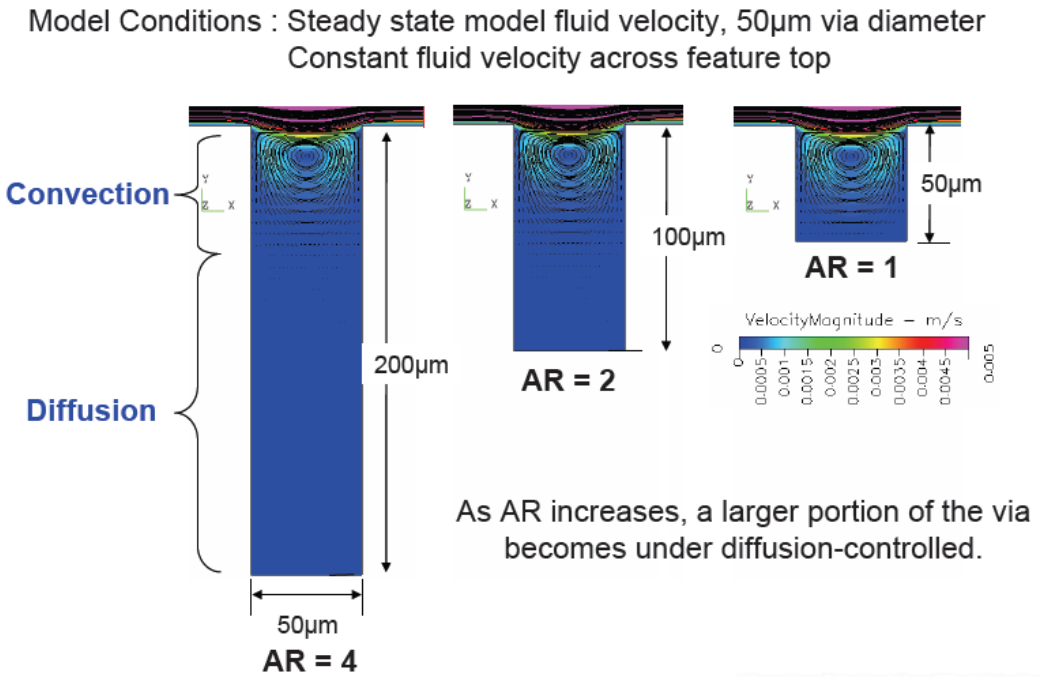

Figure 11. Theoretical calculation [5]

In VCP equipment with sparger systems there are different possibilities for the flow of the electrolyte. Three different possibilities are shown in the 12, 14 and 16.

Sparger Flowrate Profile (use of high flowrate)

Higher flow pressure can enhance the solution exchange inside the micro-via especially at the bottom or the deep via. Higher flow pressure is required for the BMV with poor laser drilling, the solution exchange is generally poor with overhang or glass fiber protrusion. It may cause the strong solution turbulence inside the micro-via that cause the unstable diffusion layer of the electroplating chemistry. The brightener or the accelerator may be “washed” away and cannot perform the bottom-up copper plating. At the same time, the leveler flush into the micro-via (as well as the surface copper) that suppress the copper growth inside the micro-via. The excessive flow rate may cause larger dimple.

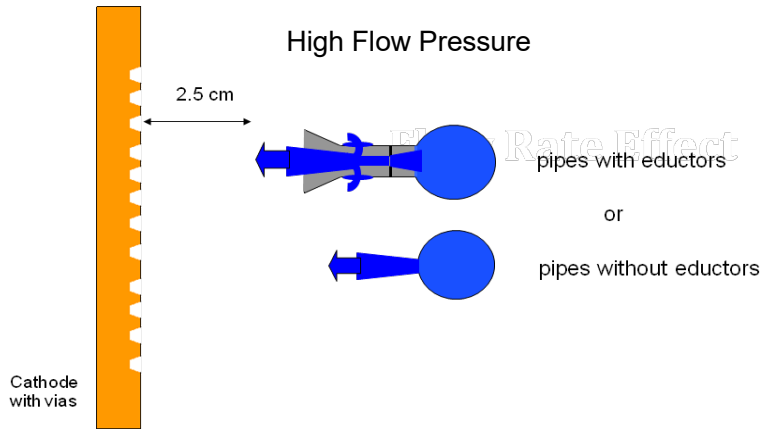

Figure 12. Sparger system face towards board with high flow pressure

Extremely high solution flow perpendicular to the surface exchanges the solution (in especially the bigger) vias resulting in half filling (see figure 13)

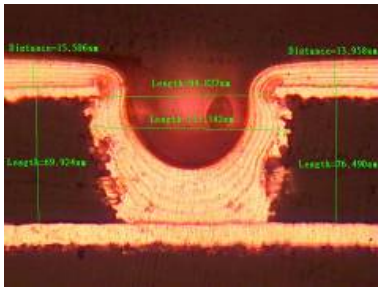

Figure 13. Half filling

Sparger Flowrate Profile (use of low flowrate)

Low flow pressure can provide more stable diffusion layer of electroplating chemistry, the brightener or the accelerator is more stable inside the micro-via, attach to the hole wall and give bottom-up copper plating. Low flow rate is highly recommended for PTH with conductive polymer. It is more suitable for the larger diameter micro-via, as the solution exchange is easier. If flow rate increases, the brightener in the diffusion layer will become unstable which lead to less bottom-up plating and larger dimple. Low flow pressure system is more suitable to used after the via is partially filled.

To get lower flow rate two different positions of the sparger system are possible. Both ways are shown in the next figures. In figure 14 the sparger system is orientated away from the cathode.

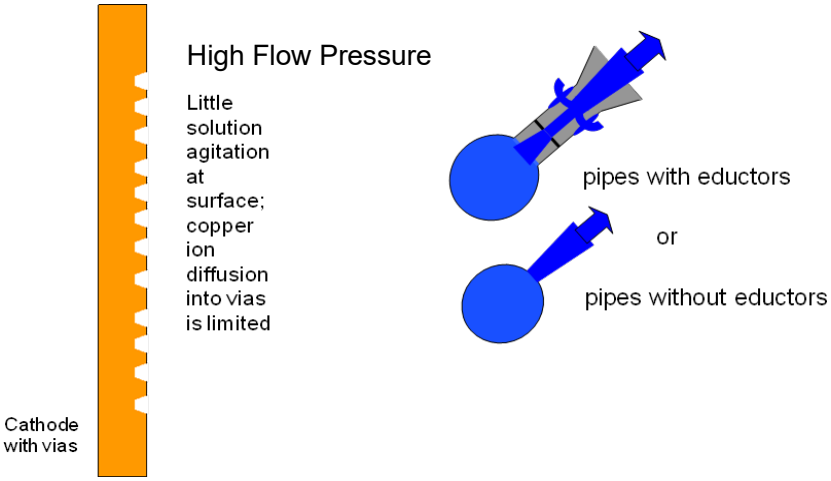

Figure 14. Sparger system face opposite to board with high flow pressure

Pipe openings turned away from surface resulting in good fill, but center / top voids (see figure 15).

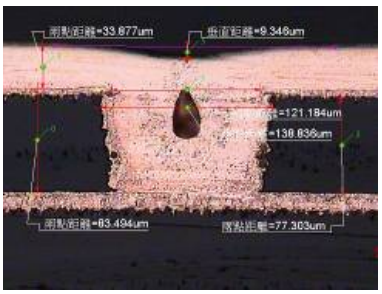

Figure 15. Small void found in micro-via filling

In figure 16 the sparger system is orientated perpendicular to the cathode but the flow rate of the electrolyte is reduced.

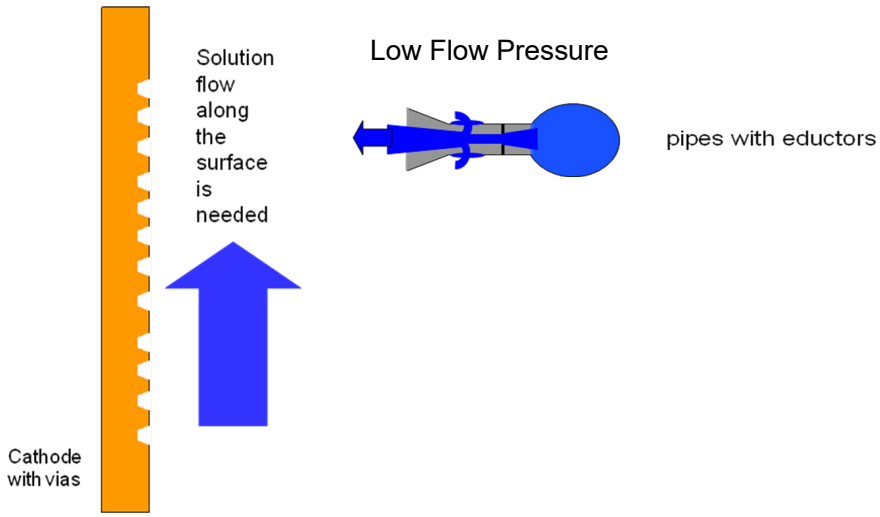

Figure 16. Sparger system face towards board with low flow pressure

Air agitation would have supplied the right solution flow along the surface or eductors with low flow pressure. This does not add fresh leveler into the vias and provides good copper ion diffusion into them (see picture 17).

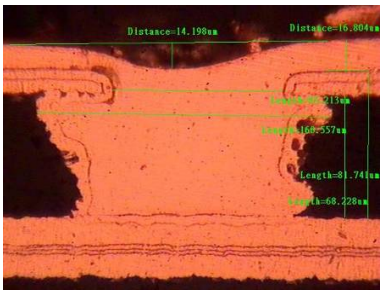

Figure 17. Good blind micro-via filling

Current Density Effect

After the hydrodynamics effect on the plating there was also a look at the effect of the current density on the copper plating. The current density effect was studied for the measured units, dimple size, overburden and grade of filling. As dummy size of the blind micro-vias the size of 100 µm in diameter and 90 µm in depth is chosen. For this feature the plating time from 30 to 100 min was taken. The checked current density window is from 1 to 2.5 ampere per square decimeter (ASD). In the figure 18 the grade of filling is shown.

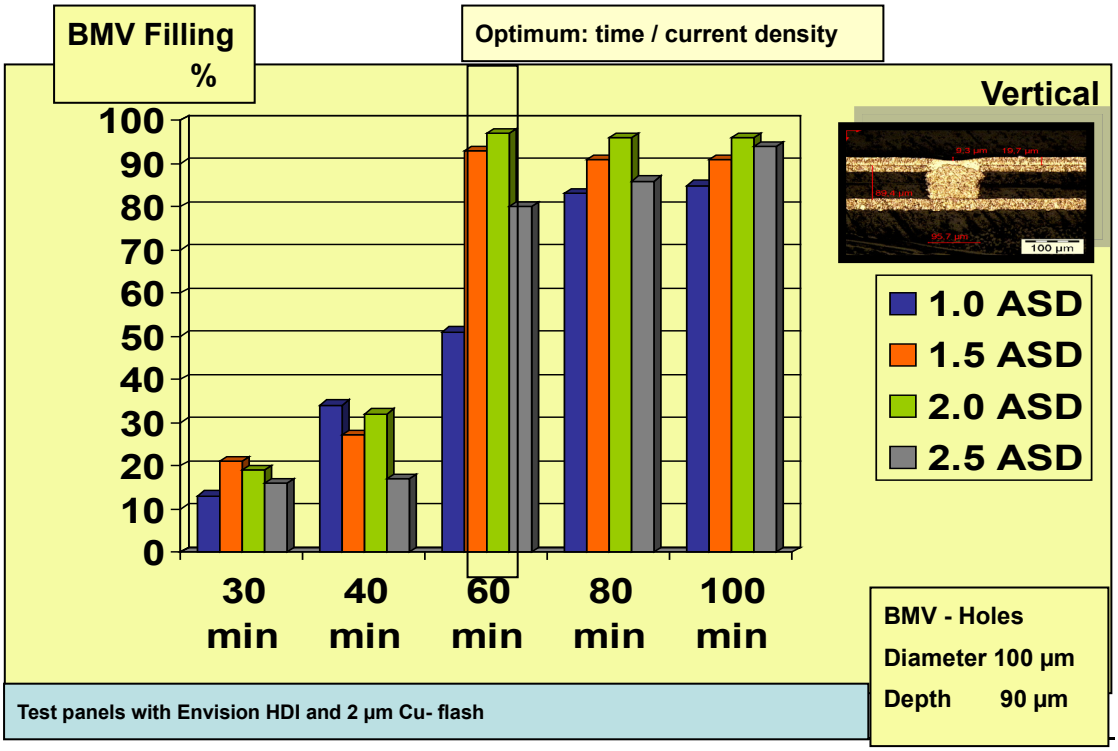

Figure 18. Time/Current vs Filling Efficiency

The outcome here is that there are two groups of current densities. The first group is with 1 ASD and 2.5 ASD where by increasing plating time the grade filling is increasing. This means at 100 min there is the highest grade of filling. The best plating time of 100 minutes is too high for a reasonable production.

To the second group belongs 1.5 and 2 ASD. Here you have up to 60 min a strong increase in grade of filling. After the 60 min the degree of filling is nearly unchanged. For the degree of filling of 100 µm by 90 µm the best conditions are at 1.5 to 2 ASD and 60 min plating time.

The figure 19 shows the effect of current density and plating time on the overburden (Copper thickness on top).

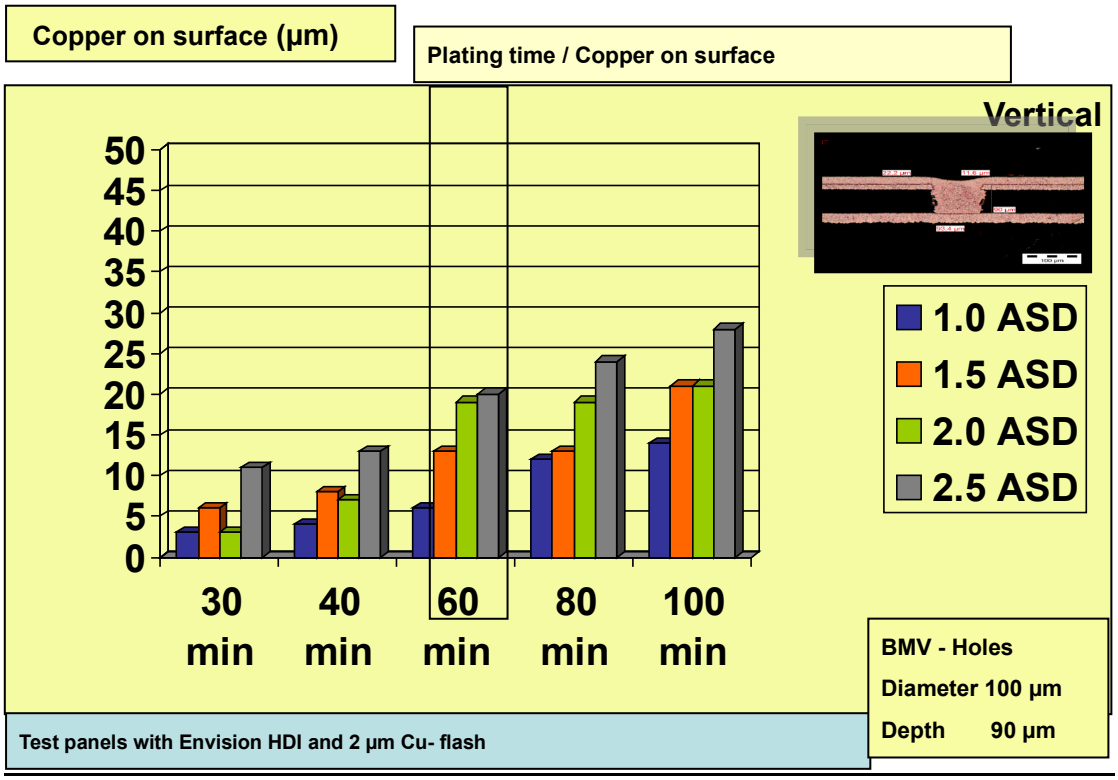

Figure 19. Time/Current vs Overburden

The overburden has independent from the current density a linear increase with time. This means e.g. at 1.5 ASD after 30 min the overburden is 6 µm and after 60 min around 12 µm. Taking now in consideration that 20 µm is the maximum overburden which is allowed the maximum plating time should be 60 min.

The figure 20 shows the effect of current density and plating time on the dimple size.

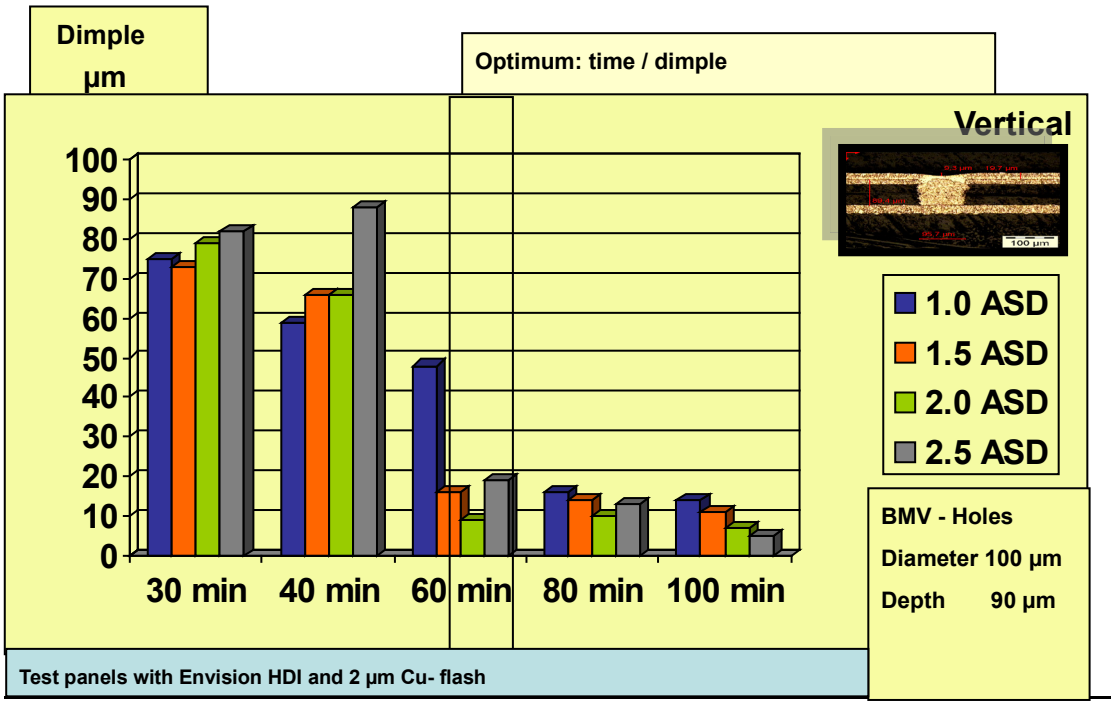

Figure 20. Time/current vs Dimple size

The dimple size is decreasing by increasing the plating time. In the case of 1.5 and 2 ASD the benefit of dimple reduction above 60 min is compare to less production capacity low. Further interesting at 60 min is that 1.5 and 2 ASD form the lowest dimple. Thereby 2 ASD gave the best result of all at 60 min. The others are following in the order of 1.5, 2.5 and at least 1 ASD.

Based on the results of the three parameters looked at these trials showed that for the blind micro-via size of 100 µm by 90 µm the best plating conditions due to time and current density were 60 min and 1.5 to 2 ASD.

Conclusion

An advanced super-filling technology which was developed in the combination with green PTH eliminate additional flash copper plating, which could minimize the use of copper as well as shorten the total process cycle time by more than 50%. Besides, the extraordinary coverage of conductive polymer over glass and resin surpass the traditional electroless copper performance; thus enhance the current flow for the micro-via and minimize the risk of plating cavity. In addition it eliminates the use of formaldehyde, heavy metal and chelating agent, as well as a more simplified process flow. In the end, it results in less hazardous waste production and water consumption. Typical two step via-filling process with additional flash copper seed layer is necessary for adsorption of accelerator to the plating surface. This innovative super-filling system does not require a copper seed layer in prior, whereas the conductive polymer initiate the growth of copper in which the adsorption/desorption of the inhibitor/accelerator system can take place. The super-filling performance will be controlled by additive ratio, hydrodynamic of the tool as well as the current profile. The via-filling plating time can be reduced to less than 60 mins with overburden at no more than 20 um whereas the micro-via aspect ratio close to 1:1.

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