

# PILOT PRODUCTION OF HIGH EFFICIENT METAL CATALYZED TEXTURED DIAMOND WIRE SAWN MC-SI SOLAR CELLS COMBINED WITH NICKEL-COPPER PLATED FRONT CONTACT PROCESSING

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**ABSTRACT:** This paper presents results of combining two promising future technologies: i) metal catalyzed textured diamond-wire sawn (DWS) mc-Si wafers and ii) nickel-copper-silver (Ni/Cu/Ag) plated front contact processing. Results of optimizations of laser patterning, annealing and module string soldering are presented. Several 60-cell module with a power output of around 270 W were made, along with subsequent generation of module reliability data. All module tests have been passed within the existing boundaries. The pseudo fill-factor (pFF) and the open circuit voltage  $V_{oc}$  has been identified as the parameter with the highest potential for further improvements. First successful results of plating-emitter development on a MCT-surface are presented.

**Keywords:** Cu plating; Light-induced plating; Diamond-wire saw, multicrystalline silicon, metal catalyzed texture

## 1 INTRODUCTION

In the past decade, the PV industry undertook considerable efforts to make Si solar cells cost effective relative to conventional carbon emitting energy generation technologies (coal, gas etc.). This goal has been achieved for several regions in the world [1]. Now, due to production overcapacity, the continued and increased pressure to further reduce production costs is driving all promising innovations (both disruptive and evolutionary). One important innovation step in the past year was the replacement of slurry-wire-based wafer sawing technology with diamond-wire-based wafer sawing technology for cast multi-crystalline (mc-Si) wafers. Amongst other improvements, this was one main step to improve the cost advantage of mc-Si wafers compared to Cz-Si wafers. On one hand, many solar cell producers are switching their production from mc to Cz wafer based silicon solar cells, because wafer costs per watt currently favour Cz Si wafers [2]. On the other hand, different approaches are being investigated to cost-effectively texture diamond wire sawn (DWS) mc-Si wafers. The common acidic HNO<sub>3</sub>/HF-based texture process, optimized for slurry-wire sawn mc-Si wafers, cannot be applied to DWS mc-Si wafers without efficiency losses in reflexion and cell-efficiency. One very promising approach is the so-called metal catalyzed texturing (MCT) technology. Its process details, electrical performance and feasibility for combination with Ni/Cu/Ag-plating are discussed in detail in the following sections.

A second very promising approach to significantly reduce production costs is the substitution of cost-intensive screen-printed Ag pastes with Ni/Cu/Ag plating [3, 4]. Furthermore, copper plating technology comes along with a

potential to increase the efficiency by 0.1 to 0.3% absolute compared to the current screen-printing technology. Due to silver's roles as both a semi-precious investment metal and as an industrial commodity, silver paste prices are highly sensitive to volatile speculative trends in metals exchange markets, which in turn has the undesirable effect of shrinking the already narrow margins of most solar cell manufactures. Replacing the Ag paste with a low-cost price-stable plated Ni/Cu/Ag stack would alleviate this cost pressure. Another important consideration is that due to the limited known reserves of silver, it will certainly become a bottleneck in the scale-up of the PV technology as it seeks to play a more significant role in the global power generation market [5]. Last, but not least, a copper-plated silicon solar cell would fit the broader commercial market's demand of abandoning lead, a toxic component of silver metallization pastes, from the device.

Thus, the two most cost-intensive factors in Si-mc-wafer-based solar cell production (wafer and metallization) are addressed by the work presented.

## 2 PROCESS AND EQUIPMENT

### 2.1. Solar cell processing

The following process flow was applied to all solar cells subsequently described herein: After obtaining wafers by diamond-wire sawing of the cast mc-Si ingot, an MCT surface texturing process as depicted in Fig. 2 was applied. The MCT process is discussed in more detail in Section 2.2. Next, a shallow 80-Ω/sq phosphorus-doped emitter was formed via thermal diffusion of POC13 (see Fig. 5, SOP). After this, PSG is etched from the cell surfaces and the junction is isolated by a single-side silicon etch. Then, a SiN<sub>x</sub> anti-reflection coating

was deposited by tube PECVD on the front side. On the rear side, Al paste (for Al-BSF formation) and silver pads (for cell inter-connection) were printed and fired for all Ni/Cu/Ag contacted solar cells. For the reference cells, a Ag paste was screen-printed on the front side before firing. This comparison of metallization process flows is illustrated in Fig. 1.

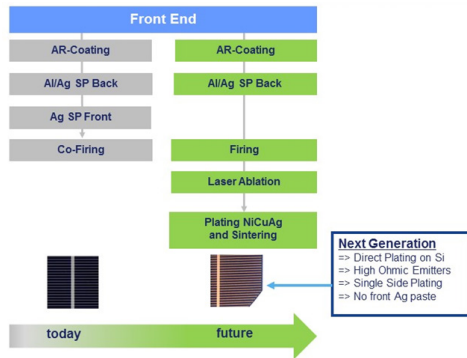


Figure. 1. Process flow overview for conventional solar cells with screen-printed silver front-side contact metallization (left) and solar cells with laser-patterned, plated Ni/Cu/Ag contact metallization, and sintering (right).

## 2.2. Metal-catalyzed texturing of diamond-wire sawn multi-crystalline Si-wafers

The process flow for metal-catalyzed texturing of diamond-wire sawn multi-crystalline Si wafers is shown in Fig. 2a.

- a)  ① alkaline DRE
-  ② MCA texture
-  ③ acidic DRE
-  ④ alkaline clean
-  ⑤ acidic clean

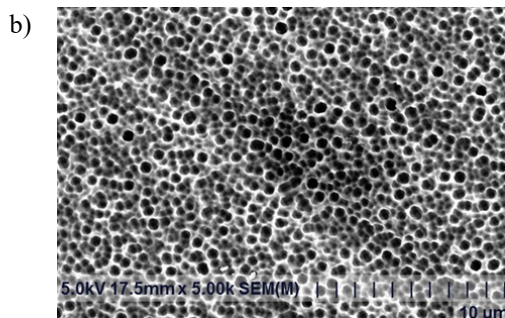


Fig. 2. (a) Process overview for the MCT process. (b) Representative image of MCT-textured DWS mc-Si wafer surface.

First, the DWS mc-Si wafers are treated with an alkaline damage-removal etch (DRE), followed by the actual MCT process, which can be sub-divided into a metal deposition step and an acidic etching step [6, 7]. Next, an acidic damage removal step is applied, followed by an alkaline clean and then an acidic clean. In-between all process steps, a rinse needs to be conducted. Application of this process chain to DWS mc-Si wafers results in surface morphologies as shown in Fig. 2b.

## 2.3. Ni/Cu/Ag plating process

In order to deposit Ni/Cu/Ag-plated contacts, the contact pattern needs to be formed by selective UV ps laser ablation (InnoLas Solutions GmbH) of the front PECVD  $\text{SiN}_x\text{:H}$  layer. The subsequent in-line plating relies on single-sided wet chemical processing in order to protect the rear contacts of the solar cells (InCellPlate, RENA Technologies GmbH). The in-line plating process starts with a chemical pre-treatment of the laser-opened areas, to assure plating will start on the exposed emitter surface where intended. Nickel (Ni) is plated by light-induced plating (LIP). A Cu layer is then plated on top of Ni, to give the contacts sufficient conductivity (see Fig. 3b and 3c). At the end of the plating sequence, single-sided immersion plating of Ag caps the Cu layer. This very thin (100 nm or less) Ag layer prevents Cu oxidation and facilitates soldering of interconnection ribbons to the metal stack (see Fig. 3a). The laser step was performed on an Innolas tool and all plating steps were performed with RENA-manufactured in-line equipment in conjunction with MacDermid-Enthone-produced plating chemistry. Intermediate rinsing and drying steps are applied in-between all process baths. In a last processing step, the complete metal stack is thermally annealed in an inert atmosphere. During this step, the adhesion of the metal stack to Si is improved and the contact resistance and line resistance are reduced via appropriate nickel silicide formation at the nickel-silicon interface [8].

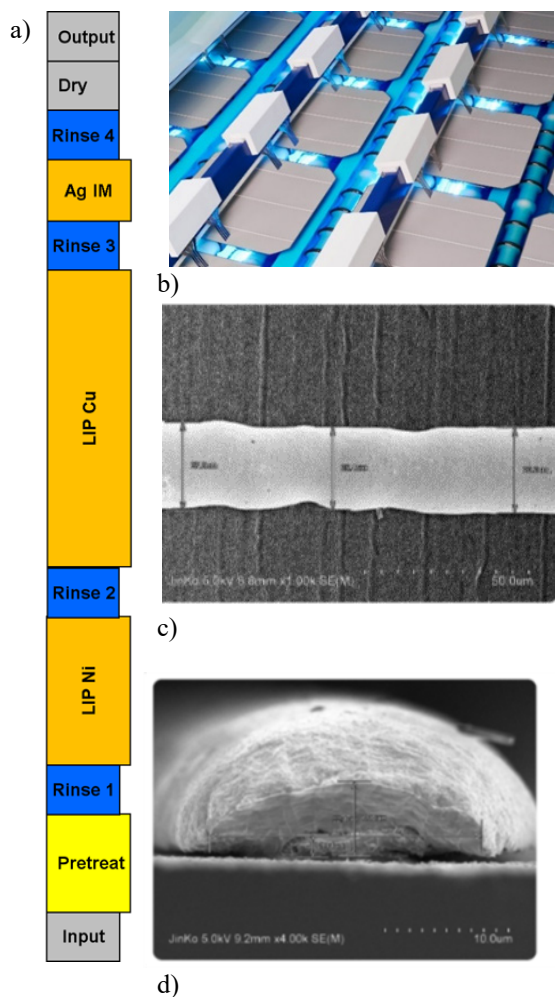


Fig. 3. (a) Sketch of Ni/Cu/Ag plating process flow; (b) picture of light-induced plating LIP Cu process bath; (c) representative SEM image of plated contact finger on a MCT DWS-Si-wafer. Left: Top view of a 22  $\mu\text{m}$  wide finger is shown. Right: Cross-section of the same contact finger with a finger height around 10  $\mu\text{m}$  is shown.

### 3 EXPERIMENTAL WORK

In order to achieve an efficiency increase with plated cells relative to Ag-paste screen printed cells, some process steps have to be individually optimized [9].

#### 3.1. Laser processing and influences on solar cell performance

First, the laser process was optimized to the MCT wafer surface. The goal is to realize a homogenous opening in the  $\text{SiN}_x$  layer while simultaneously minimizing the creation of a laser-induced damage region (specifically, silicon amorphization) within the emitter's crystal structure. In Fig. 4a, mean efficiency values (5 cells per group) before and after annealing are shown over varied laser pulse energies. A wide process window, between 0.6 to 0.8  $\mu\text{J}/\text{pulse}$ , results in high efficiencies of above 19%. No significant

difference in the investigated dependence can be distinguished before and after the anneal process, aside from an increase in efficiency by approximately 0.2%. In Fig. 4b, a representative surface image after laser patterning is shown for the optimum laser parameter of 0.8  $\mu\text{J}/\text{pulse}$ .

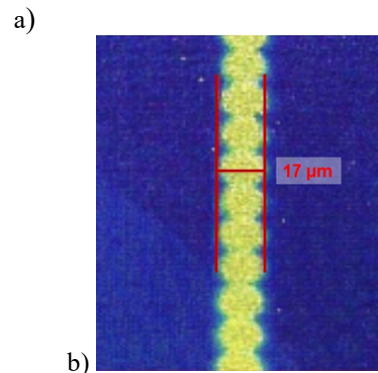
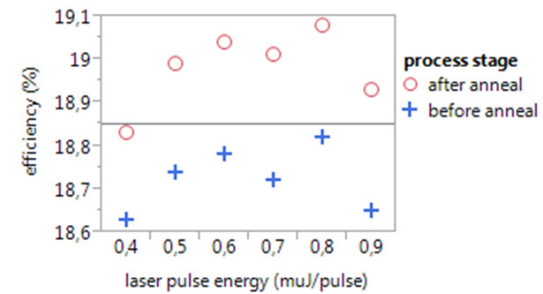


Fig. 4. (a) Mean efficiency values (5 cells per group) before and after annealing over normalized laser power is shown. (b) Representative surface image after laser patterning.

#### 3.2. I-V data comparison of MCT mc-Si solar cells contacted by silver paste screen-printing vs. Ni/Cu/Ag-plating

After the initial process development (process 'base-lining') cycle, as described in Sections 3.1, two groups (10 cells each) of cells are fabricated in order to compare the electrical performance of the plated Ni-Cu-Ag contact technology to conventional screen-printed Ag paste contact technology. The I-V data is shown in Table 1. The efficiency for the plated front contact group is slightly higher. The main reasons for this are a superior short circuit current ( $J_{sc}$ ) and FF. The higher FF is mainly explained by a significantly reduced series resistance ( $R_s$ ) value. Based on the observed  $R_s$  difference, an even higher advantage in FF should be observed [11]. Based on this observed difference, it is reasoned that the plated group has a reduced pseudo fill factor. This finding leads to the conclusion that the diode quality of the plated cells is most likely reduced either by a laser-induced emitter damage, a too-shallow junction, Ni-silicide spiking after anneal, or a combination of the above-mentioned influences. Furthermore a 5 mV lower  $V_{oc}$  value is observed for the plated contact group.

Table 1. Overview of I-V data (efficiency,  $V_{oc}$ ,  $J_{sc}$ , FF and  $R_s$ ) for two different front contact metallization: i) Ni/Cu/Ag plating (after annealing), and ii) Ag-paste screen printing. The group size is 10 cells per group.

Group	$\eta$ (%)	$V_{oc}$ (mV)	$J_{sc}$ (A)	FF (%)	$R_s$ (m $\Omega$ )
Ni/Cu/Ag plated					
MCT cells	19.04	637	9.11	80.37	1.3
Ag screen printed					
MCT cells	19.00	642	8.99	80.12	2.1

Both, the reduced pFF and  $V_{oc}$  value are treated with an emitter profile adaptation approach. A first approach of a plating emitter created on a MCT-wafer is shown in Fig.1. A standard operation procedure (SOP) emitter (optimized for Ag-paste technology) is shown as a reference. It is believed that a deeper junction can increase the junction quality by reducing Ni-spiking and sensitivity to laser damage.

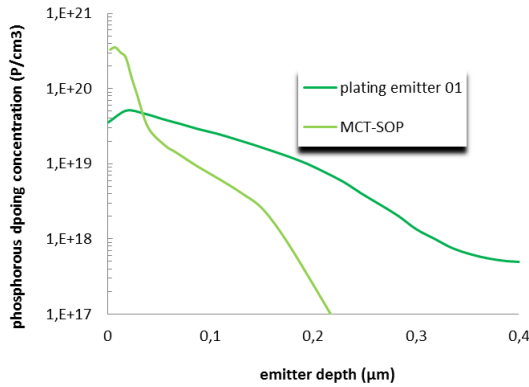


Fig. 5: Phosphorous profile of a typical industrial standard operation process (SOP) emitter (dark green) and first approach for an emitter adapted for plating contacts (light green).

Two groups of MCT-SOP mc-Al-BSF solar cells have been processed with the emitter depicted in Fig. 5. The MCT-SOP emitter cells have been contacted by optimized Ag-paste screen print technology. The -plating emitter 01- mc-Al-BSF solar cells have been processed with the emitter depicted in Fig. 5. The plating-emitter-01 cells have been contacted by the plating technology. The IV-data results are summarized in Tab.2. On the one hand, the gap in  $V_{oc}$  could be closed. On the other hand some difficulties in solar cell processing resulted in inferior  $V_{oc}$ , FF,  $R_s$ , and  $\eta$  values, compared to the data presented in Tab.1.

Future work will aim for further improvement of the plating emitter in order to increase the pFF-value and close the  $V_{oc}$ -gap simultaneously.

Table. 2: IV data measured for MCT mc-solar cells processed with special emitter profiles (show in Fig 5) for plating and Ag-screen print contacts.

group	no.	mean $\eta$ (%)	$V_{oc}$ (mV)	$I_{sc}$ (A)	FF (%)	$R_s$ (m $\Omega$ )
Ni/Cu plated standard emitter	26	18.75 +/- 0.1	637 +/-1	9.11 +/- 0.03	79.35 +/-0.2	2.2 +/-0.2
Ag printed, standard emitter	31	18.78 +/- 0.1	637 +/- 1	9.05 +/- 0.03	80.07 +/- 0.4	1.7 +/- 0.2

#### 4. MODULE RESULTS

Before committing to the fabrication of a pilot production of 1<sup>st</sup> 50, and 2<sup>nd</sup> 200 full-sized 60-cell modules, the feasibility of Ni/Cu/Ag-plated MCT mc-Si cells to standard solder technology for interconnecting 12 cells in a string is investigated. In Fig. 6, the observed failure pull strength forces, after standard module-production contact tab soldering is performed, are shown. All values were determined under a pull angle of 60°. The contact annealing temperature and time was varied from 300°C to 450°C and 3 min to 6 min, respectively. Values above 1 N are known to enable a reliable module production process. Longer annealing times perform slightly better compared to the 3 min anneal, with most values well above 2 N. Further, optimization of the soldering process will be part of future experiments.

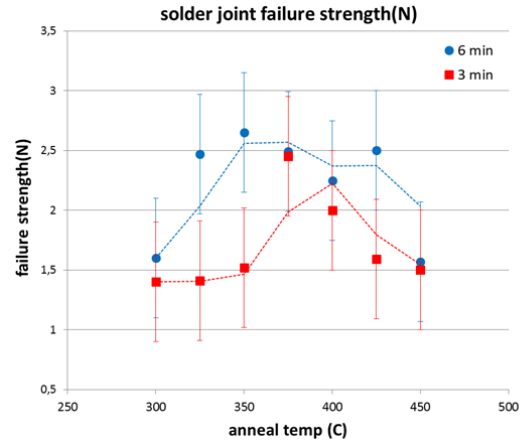


Fig. 6. Measured failure pull strength force after standard contact tab soldering for module production. All values were determined under a pull angle of 60°. The contact annealing temperature and time were varied from 300°C to 450°C and 3 min (red) to 6 min (blue), respectively.

After obtaining positive results, as discussed in Section 3.3 and shown in Fig. 6, more than 2000 MCT cells were fabricated and contacted by the plating technology (please see I-V data distribution and further statistical information in Fig. 8a) with a mean  $\eta$  of 18.84%. As a reference, more than 10000 MCT cells from the same production-batch

were processed and contacted by standard Ag-paste screen print with a mean  $\eta$  of 18.79% (see I-V data distribution and further statistical information in Fig. 8b). Thus, in the presented experiment an efficiency gain of 0.05% could be observed. Typical efficiency gain values range around 0.1% at an efficiency level above 19%.

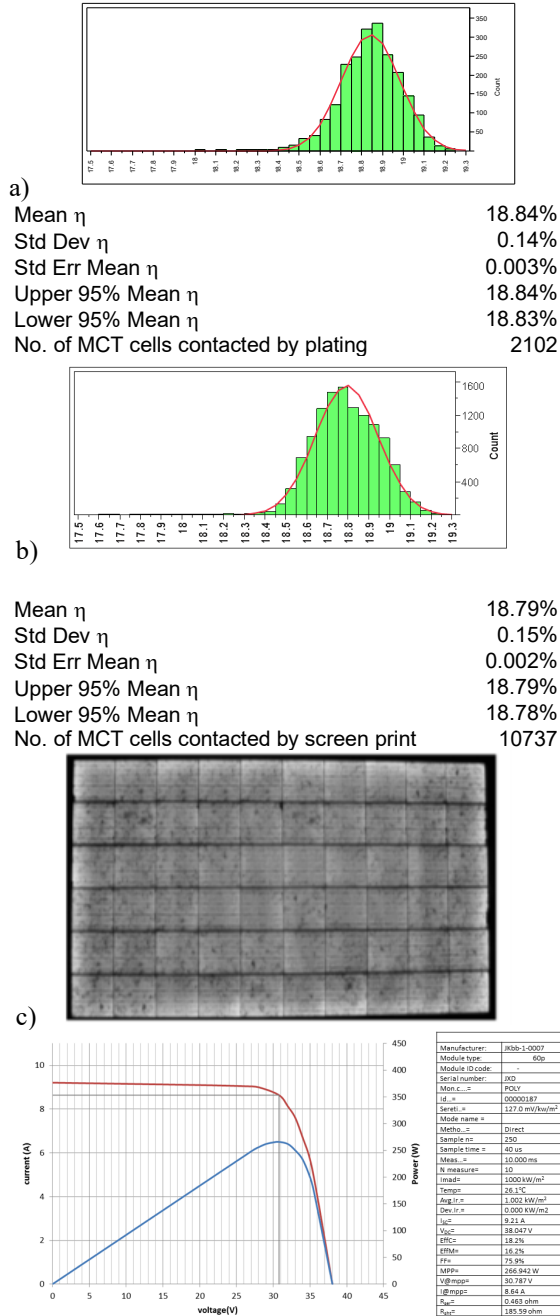


Fig. 7. (a) Efficiency binning distribution of 2102 MCT mc-Si solar cells contacted by a plated Ni/Cu/Ag stack. (b) Efficiency binning distribution of 10737 MCT mc-Si solar cells contacted by Ag-screen print. (c) EL image and (d) I-V data of a representative 60-cell module populated with cells.

Several 60-cell module were subsequently manufactured and tested for long term stability thermal cycling and humidity freeze testing. All module tests have been passed within the existing boundaries. A representative module's electro-luminescence (EL) image is shown in Fig. 8c. Please note that despite no adaptation of the cell interconnection or the module 'lay-up' processes to the presence of plated bus bar pads, neither cell cracks, nor finger interruptions, nor other typical module failure modes are observed through visible inspection of the EL image. The module I-V data is shown in Fig. 8d. The power output is 266 W. After completion of further optimization loops, modules in the output range of 280 to 290 W are expected.

### 5. Cz-PERC SOLAR CELL RESULTS

As a side project the plating technology has been applied to standard industrial Cz-PERC solar cells. The same efficiency of 21.3% could be observed for the Ni/Cu/Ag plated as well as for the Ag-paste screen printed group. The slightly lower  $V_{oc}$ , FF and  $R_s$  values for the plated group is compensated by a superior  $I_{sc}$  value (see Tab. 3).

Table 3: IV-data of industrial production Cz-PERC solar cells contacted with Cu-plating and Ag-paste screen print.

group	no.	$\eta$ (%)	max $\eta$ (%)	$V_{oc}$ (mV)	$I_{sc}$ (A)	FF (%)	$R_s$ (m $\Omega$ )
plated Cz PERC	49	21.3 +/- 0.1	21.5	662 +/- 1	9.89 +/- 0.02	79.5 +/- 0.2	2.5 +/- 0.1
printed Cz PERC	200	21.3 +/- 0.1	n.a.	665 +/- 1	9.81 +/- 0.02	79.6 +/- 0.2	2.4 +/- 0.1

### 5. CONCLUSION AND OUTLOOK

In this paper, we show that combining two emerging technologies - metal catalyzed textured diamond wire sawn mc-Si wafers and Ni/Cu/Ag-plated front contact processing - show very good results, even at the process 'base-lining' stage of development. Results from the initial pilot production and process optimization, including laser patterning, annealing, and soldering are presented.

Several 60-cell module with a power output around 270 W were made, along with subsequent generation of module reliability data. All module tests have been passed within the existing boundaries. Since unit process development and whole process integration are in the early stages, it is expected that further optimizations will result in rapid improvement of the cell and module performance.

As a primary case-in-point, discussed in Section 3.2, it is noted that the plated cell's I-V response mainly suffers from a reduced pFF and

$V_{oc}$ . A very promising solution for this is moving away from an emitter profile which is mainly optimized for silver paste's restricted sintering parameters (and thus is limiting the contacting properties) and, instead, developing an optimized emitter profile suited for highly-ohmic Ni/Cu/Ag-plated contacts. First successful results of plating-emitter development on a MCT-surface have been presented. Future work will continue to focus on further emitter profile adaptation, evaluation of selective emitter technology and continuous efficiency improvement.

## 9 REFERENCES

- [1] Lazard. Lazard's levelized cost of energy analysis – Version 10.0. 2016. [www.lazard.com/media/438038/levelized-cost-of-energy-v100.pdf](http://www.lazard.com/media/438038/levelized-cost-of-energy-v100.pdf).
- [2] SEMI PV Group Europe 2016, ITRPV Eight Edition 2017, [www.itrpv.net/reports/downloads/\(10.4.2017\)](http://www.itrpv.net/reports/downloads/(10.4.2017)).
- [3] Horzel J, Shengzhao Y, Bay N, Passig M, Pysch D, Kühnlein H, Nussbaumer H., Verlinden P. Industrial Si solar cells with Cu-plated contacts. *IEEE J. Photovolt.* 2015; 5(6):1595-1600.
- [4] Shi Z, Wenham S, Ji J. Mass production of the innovative PLUTO solar cell technology. *Proc. 34<sup>th</sup> IEEE Photovoltaic Specialists Conference (PVSC), 2009.* DOI: 10.1109/PVSC.2009.5411566.
- [5] Meng T. *Terawatt Solar Photovoltaics: Roadblocks and Opportunities.* Springer Verlag 2014, DOI 10.1007/978-1-4471-5643-7.
- [6] Ye X, Zou S, Chen K, Li J, Huang J, Cao F, Wang X, Zhang L, Wang X, Shen M, Su X. 18.45% Efficient Multi-Crystalline Silicon Solar Cells with Novel Nanoscale Pseudo-Pyramid Texture. *Adv. Funct. Mater.* 2014; 6708–6716.
- [7] Wang X, Zou S, Xing G. 19.31% efficient multicrystalline silicon solar cells using MCCE black silicon technology. *Photovoltaics International 35th Edition.* 02/2017.
- [8] Russel R, Tous L, Philipsen H, Horzel J, Cornagliotti E, Ngamo M, Choulat P, Labie R, Bekcers J, Bertens J, Fujii M, John J, Poortmans J, Mertens R. A simple copper metallization process for high cell efficiencies and reliable modules. *Proc. 27th EUPVSEC, Germany, 2012.*
- [9] Bay N, Brand A, Büchler A, Burschik J, Kluska S, Kühnlein HH, Passig M, Pysch D, Sieber M. Benefits of different process routes for industrial direct front side plating. *7th International Conference on Silicon Photovoltaics. SiliconPV 2017.*
- [10] Murakami T, Froment B, Ouaknine M, Yoo W. Nickel silicide formation using a stacked hotplate based low temperature annealing system. *203rd Electrochemical Society Meeting, Paris, 2003.*
- [11] Pysch D, Mette A, Glunz SW. A review and comparison of different methods to determine the series resistance of solar cells. *Sol. Energy Mater. Sol. Cells* 2007; 91:1698–1706.

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